|| Volume 5 || Issue 8 || August 2020 || ISSN (Online) 2456-0774
INTERNATIONAL JOURNAL OF ADVANCE SCIENTIFIC RESEARCH
AND ENGINEERING TRENDS

DESIGN OF LOW POWER AND AREA EFFICIENT MULTIPLIERS USING ADVANCED GDI METHOD

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Abstract: Today, more and more, high speed mobile computational devices and equipments are being introduced in the market. These computational devices strain and drain the battery very quickly. Researchers are making efforts to find ways and means to conserve the battery power for longer period. The core key components in these computational devices are the Multipliers to support high speed computational intensive applications in real time. Thus it becomes more important to reduce power dissipation and area in these multiplier modules as they affect the performance of the device. Several VLSI design techniques have been attempted to optimize the power and area occupied by the multiplier module, but there are very few design techniques that gives the required extensibility both in terms of power and area. In this paper a high speed, reliable and efficient multiplier VLSI module design is presented using GDI (Gate Diffusion Input) technique, addressing both power consumption and area complexity. Further, comparative study results of the proposed design over the traditional CMOS design are also presented. Detailed design steps and comparative study using Tanner simulation tool at 25nm CMOS technology is discussed. The simulation results presented show reduction in both power and area of the proposed design compared to state of art approaches.

Keywords: *GDI, FA, MULT*

I INTRODUCTION

The multiplier finds its usage in practically all kinds of processing systems ranging from application specific processors dealing with an infinitely large bit width or a small scale general processor dealing with a comparably smaller subset of data. It also happens to be one of the most time-consuming digital processes and offers a good scope for improvement in terms of area, delay as well as power efficiency. The conventional hierarchical array multiplication is a simple looped method of binary multiplication in which a multiplicand is repetitively multiplied with individual bits of second multiplicand and the partial product terms are then finally added to yield the product. The process, however simple in approach and implementable hierarchically, requires extensive hardware and is also marred by a heavy adder delay. The adder delays are often tackled with complex adder systems that in turn increase the hardware requirements of the system along with the inherent delay. We aim to tackle these hurdles by using the ancient concepts of Vedic Mathematics. Out of the hundreds of theorems available in the arsenal of Vedic Mathematics, we aim to reduce the mathematical complexity of the binary multiplication process by using the Urdhva-Tiryagbhyam (UT) theorem. It is basically a decimal multiplication theorem which effectively simplifies the multiplication process. The UT theorem can be easily adapted to binary process as well and can be used to reduce the circuit complexity of the multiplier. The UT theorem has been proven to reduce the delay as well as power consumption of the multipliers even in the CMOS process but we further aim to optimize the area constraints as well as the power consumption of the multiplier quite effectively by using a modified circuit for the Gate-Diffusion-Input (GDI) cells. The GDI cells offer a minimalistic technique to reduce the area or the transistor count of a design by the virtue of their capability to implement complex functions in comparably fewer transistors. The use of fewer transistors also leads to fewer switching and thereby conserves a lot of switching energy as well as delay. They also have the added advantage of being easily fabricated with slight modifications to the twin-tub CMOS process.

2. Modified GDI

The GDI design technique was introduced as a promising alternative to the CMOS logic design style of complimentarily functioning gates. Originally proposed for fabrication in Silicon on Insulator (SOI) and twin-well CMOS processes, GDI methodology allows the implementation of a wide range of complex logic functions using merely two transistors. GDI implementation of a design thus helps in reducing its overall transistor count and thereby improves area constraints of the design.

Table 1: function implementation using GDI cell

N	P	G	D	Functions
0	1	A	A`	Inverter
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A`B+AC	MUX
B`	B	A	A`B+AB`	XOR
B	B`	A	AB+A`B`	XNOR

The Fig. 1. shows the basic construction of a GDI cell. We have implemented our design in 180nm technology with a Wp/Wn ratio of 3. In conventional GDI cells, the gates of the PMOS & NMOS devices are shorted to yield an input G, the sources terminals are individually shorted with the substrate to yield the P&N terminals respectively for PMOS & NMOS. This simple configuration of mere two MOS devices is capable of producing many complex logic functions as shown in the TABLE 1. We thus get a general idea about how advantageous it is to use GDI cells in place of the conventional CMOS logic implementations. However, there"s a certain caveat of partial swing in GDI cells which renders them practically unusable for any cascade connection with other gates. It also leads to wild harmonics in the output signals which dissipate more power than saved. Hence, the actual utility requires a few modifications to the basic GDI cell design as evident in the Fig. 1. while the functionality remains the same.

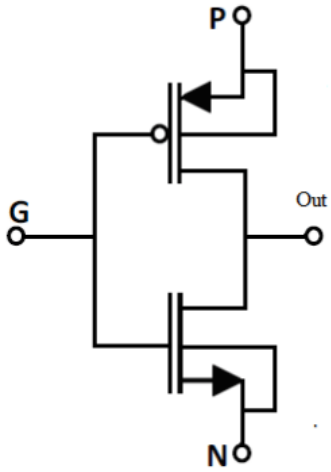

Fig. 1. A GDI cell

2.1 GDI AND GATE

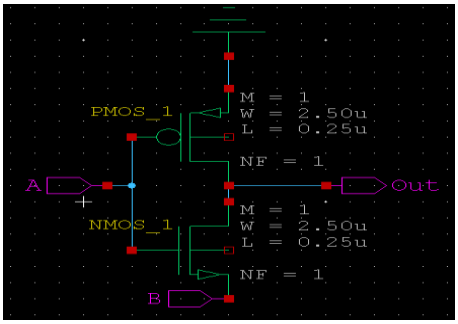

Fig. 2. GDI AND cell

Fig. 2 shows the design of an AND gate based on GDI method. It requires a single GDI cell in which the source of the PMOS that is port P is connected to GND and A is given as an input to port G while port N is supplied input B.

2.2 GDI XOR GATE

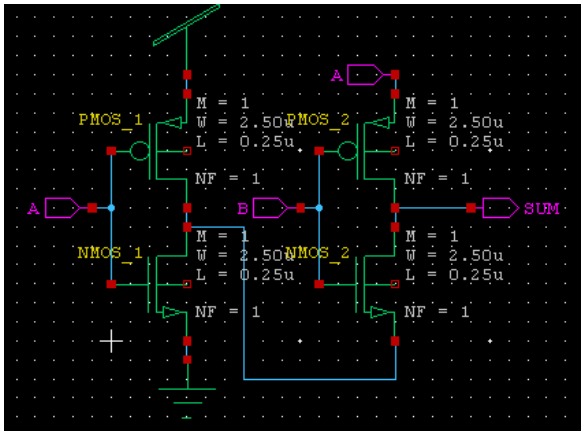

Fig. 3 GDI XOR cell

The XOR gates based on GDI cells are applications of the GDI technique. As can be seen in Fig. 3, each of them requires only four transistors. Obviously, the proposed GDI XOR and XNOR gates use less transistors compared with the conventional CMOS

counterparts. Due to some attractive features which allow improvements in design complexity, transistor counts, static power dissipation and logic level swing, research on GDI is becoming feverish in VLSI area. However, the GDI scheme suffers the defect of special CMOS process, specifically, it requires twin-well CMOS or silicon on insulator (SOI) process, which are more expensive than the standard p-well CMOS process. This challenges its applicability in many CMOS circuits.

2.3 GDI FULLADDER

The GDI XOR gate is shown as Fig. 3where only 4 transistors are used. Compare the GDI XOR with the its conventional CMOS counterpart. The transistor level implementation of GDI XOR full adder is shown in Fig. 4 and figure 5. This full adder consists of three modules— two GDI XOR gates and a multiplexer. In the worst case, Sum has 4-T delay while Cout has 3-T delay. However, due to the advantages of GDI cell, this circuit still can achieve its benefit of low power consumption. the GDI XNOR full adder which is another basic architecture of the application of GDI cells. This scheme also includes three modules. It contains two GDI XNOR gates and a multiplexer. In the worst route, Sum has 4-T delay and Cout has 3-T delay. The Sum and Cout can be calculated from (2) and (4) respectively.

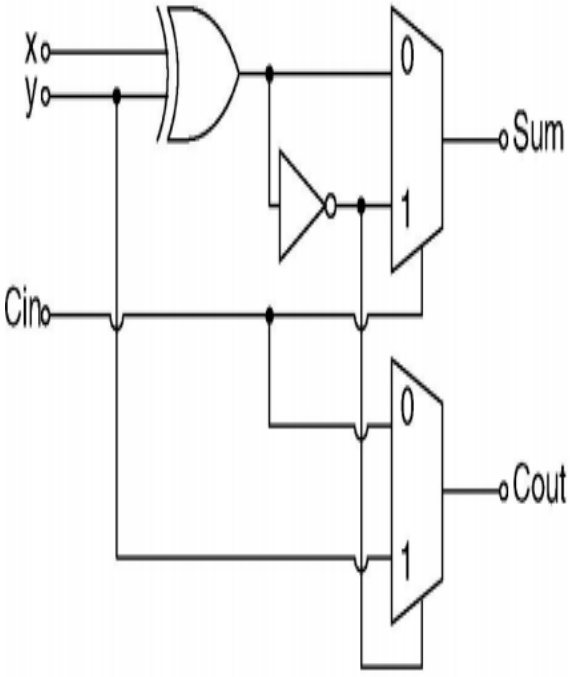

Fig. 4 Block diagram of GDI Full adder

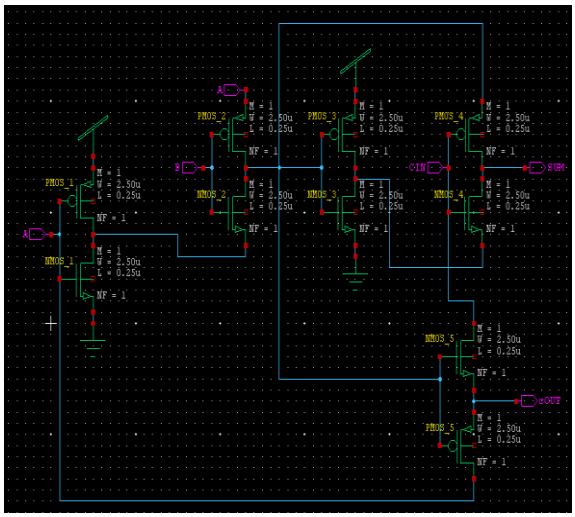

Fig. 5 Schematic diagram of GDI Full adder

III. PROPOSED ARRAY MULTIPLIER:

Array multiplier is the simplest structure of parallel multiplier. This multiplier using the standard adds and shift operation based on 'add and shift' algorithms to perform a multiplication operation. The structure of 4-bit array multiplier is presented in fig. 6. The partial products generator consists of n number of 'AND' gates to multiply the multiplicand with each bit of the multiplier and then these partial products are shifted depending on their order and this summation operation can be performed by using full adder and a half adder. In 4x4 array multiplier, 4x4 AND gates used to generate partial products and 4x (4-2) full adders and 4 half adders used to generate.

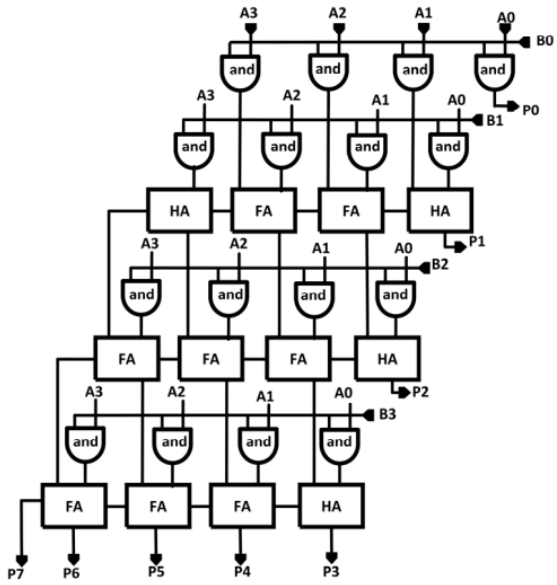

Fig. 6. 4x4 Array Multiplier

Here, the GDI based AND gates are utilized as shown in figure 3. The half adder is formed by the combination of XOR gate, AND gate. The half adder

sum will be generated by using XOR gate as shown in figure 4 and carry out will be developed by using AND gate as shown in figure 3. The Full adder utilized as shown in figure 5.

IV. SIMULATION RESULTS:

The proposed XOR, AND gates and the four low power full adders and multipliers are simulated using Tanner Tools. All the results are obtained in 25nm GDI process technology with a 1.8V supply voltage. In order to establish an impartial simulation circumstance, authors prefer the input and output patterns in Fig. 7.

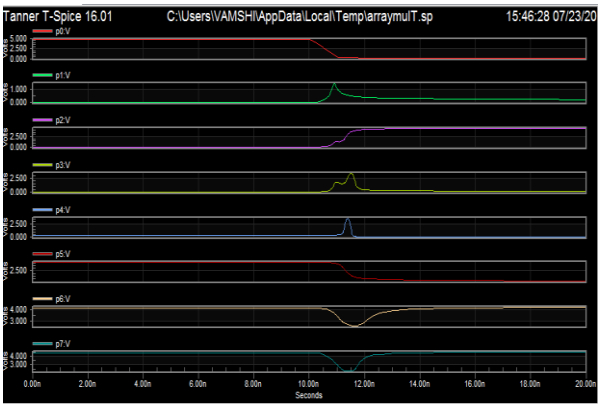

Fig. 7 Array Multiplier output

Transistor count and working speed (frequency and delay) are yardsticks for the performance of GDI circuits. These are listed in TABLE II. In order to compare the four proposed full adders with the conventional multipliers. Another important standard for CMOS circuits is Power Delay product (PDP). This parameter is applied often in testing characteristics of CMOS circuits. Since, in many cases, requirements of low power and high speed cannot be accomplished simultaneously, comparisons only using these two metrics may become problematical.

Table 2: comparison with various methods

Design	Power (uW)	Delay (pS)	No.of Transistors
Array Multiplier-CMOS	53.8	146	400
Array Multiplier-GDI	109	159	296
Array Multiplier-FSGDI	44	133	260
proposed	**6.68**	**10**	**136**

From the table it is observed that the proposed method consumes low power, area as well as low delay requirements.

V CONCLUSION:

The results obtained for the proposed multiplier effectively prove that the proposed multiplier design works better than the other designs in terms of all the parameters in comparison. The most prominent improvement achieved over other designs is in terms of the area or transistor count. The uses of Mod-GDI cells along with the shit and add theorem thus effectively reduces the area-constraints, marginally improves the speed of operation and also reduces the power consumption of the multiplier unit.

REFERENCES

[1] N. Weste, D. Harris, CMOS VLSI Design a Circuits and Systems Perspective, 4thEd, Addison-Wesley, 2011.

[2] A. Morgenshtein, A. Fish, and I. Wagner, “Gate-diffusion input (GDI): a power-efficient method for digital combinatorial circuits,” IEEE Transactions on Very Large Scale Integration (VLSI) Systems IEEE Trans. VLSI Syst., vol. 10, no. 5, pp. 566–581, 2002.

[3] A. Morgenshtein, I. Schwartz, and A. Fish, "Gate Diffusion Input (GDI) logic in standard CMOS Nanoscale process," 2010 IEEE 26th Convention of Electrical and Electronics Engineers in Israel, 2011.

[4] A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, and A. Fish, "Fullswing gate diffusion input logic—Case-study of low-power CLA adder design," Integration, the VLSI Journal, vol. 47, no. 1, pp. 62–70, 2014.

[5] Mansi Jhamb, Garima and Himanshu Lohani,"Design, implementation and performance comparison of multiplier topologies in power-delay space", Engineering Science and Technology, an International Journal, 2015.

[6] Mariano Aguirre-Hernandez and Monico Linares-Aranda," CMOS FullAdders for Energy-Efficient Arithmetic Applications", IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 19, NO. 4, APRIL 2011, 2011.

[7] Jyh-Ming Wang, Sung-Chuan Fang and Wu-Shiung Feng," New Efficient Designs for XOR and XNOR Functions on the Transistor Level", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 29, NO. 7, JULY 1994,1994.

[8] A. Shams, T. Darwish, and M. Bayoumi, "Performance analysis Of lowpower I-bit CMOS full adder cells," IEEE Trans. on VLSI Syst. vol IO, no. 1,pp.20-29, 2002.
[9] Chowdhury, S.R., Banerjee, A., Roy, A. and Saha, H;" A high speed 8 transistor full adder design using novel 3 transistor XOR gates", International Journal of Electronics and Communication EngineeringVol:2, No:10, 2008.
[10] Mohan Shoba and Rangaswamy Nakkeeran,"GDI based full adders for energy efficient arithmetic applications", Engineering Science and Technology, an International Journal, 2016.
[11] John B. Gosling, Design of Arithmetic Units for Digital Computers, 1980.
[12] Mohan Shoba and Rangaswamy Nakkeeran," Performance Analysis of 1- bit Full Adder Using GDI Logic", ICICES2014 - S.A.Engineering College, Chennai, Tamil Nadu, India,2014.
[13] E. Abu-Shama and M. Bayoumi, "A new cell for low-power adders," in Proc. Int. Midwest Symp. Circuits Syst., 1995.
[14] T. Bhagyalaxmi, S. Rajendra, S. Srinivas," Power-Aware Alternative Adder Cell Structure Using Swing Restored Complementary PassTransistor Logic at 45nm Technology", 2nd International Conference on Nanomaterials and Technologies (CNT 2014), 2014.
[15] M. Alioto, G. Di Cataldo, and G. Palumbo," Mixed Full Adder topologies for high-performance low-power arithmetic circuits", Microelectronics Journal 38 (2007) 130–139,2007.
[16] Korra Ravi Kumar, P.Mahipl Reddy, M.Sadanandam, Santhosh Kumar.A, and M.RAJU,"Design of 2T XOR Gate Based Full Adder Using GDI Technique", International Conference on Innovative Mechanisms for Industry Applications (ICIMIA 2017), 2017.
[17] Nehru Kandasamy, Firdous Ahmad, Shasikanth Reddy, Ramesh Babu M, Nagarjuna Telagam and Somanaidu Utlapalli," Performance Analysis of 4-Bit MAC Unit using Hybrid GDI &Transmission Gate based Adder and Multiplier Circuits in 180 nm & 90 nm Technology", Microprocessors and Microsystems Journal, 2018.
[18] Chiou-Kou Tung, Yu-Cherng Hung, Shao-Hui Shieh, and Guo-Shing Huang," A Low-Power High-Speed Hybrid CMOS Full Adder for Embedded System", 2007 IEEE Design and Diagnostics of Electronic Circuits and Systems conference, 2007.
[19] Mohan Shoba and Rangaswamy Nakkeeran," GDI based full adders for energy efficient arithmetic applications", Engineering Science and Technology, an International Journal, 2015.