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DESIGN OF NETWORK ON CHIP BASED CDMA ENCODER WITH WB-SB DECODERS

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ABSTRACT

On-chip interconnects are the overall performance bottleneck in contemporary system-on-chips. Code-department multiple get admission to (CDMA) has been proposed to enforce on-chip crossbars because of its fixed latency, decreased arbitration overhead, and higher bandwidth. In CDMA, medium sharing is enabled inside the code space by way of assigning a restrained quantity of N-chip length orthogonal spreading codes to the processing factors sharing the interconnect. In this project, we increase overloaded CDMA interconnect (OCI) to decorate the ability of CDMA Network-on-chip (NoC) crossbars by increasing the wide variety of usable spreading codes. Serial and parallel OCI architecture versions are supplied to adhere to one-of-a-kind place, postpone and energy necessities. Compared with the traditional CDMA crossbar, on a Xilinx Artix-7 AC701 FPGA package, the serial OCI crossbar achieves 100% better bandwidth, 31% less aid utilization, and forty five% energy saving, even as the parallel OCI crossbar achieves N times higher bandwidth compared with the serial OCI crossbar on the cost of elevated vicinity and energy intake. A 65-node OCI-based totally big name NoC is implemented, evaluated, and compared with an equivalent area department a couple of get right of entry to totally based on NoC for various artificial site visitors' styles. The evaluation effects in phrases of the aid usage and throughput spotlight the OCI as a promising era to enforce the bodily layer of NoC routers.

Index Terms:

Code-division multiple access, overloaded CDMA interconnect, Xilinx, Network-On-Chip.

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I OVERVIEW

On-chip exchanges altogether influence the overall zone, execution, and force use of present-day system on-chips (SoCs). Extending the correspondence over-head corrupts the speedup achieved by equal figuring according to Amdahl's law. As such, making efficient unrivalled on-chip interconnects has been of focal centrality for the equal and tip top figuring propels. Network on-chips (NoCs) are the most flexible interconnection perspective that is prepared for watching out for various application needs and meet particular performance requirements of generous residual jobs that needs to be done, including idleness by methods for adaptable coordinating, throughput by methods for improved way jumper sity, control dispersal by smoothing out the NoC to centred remarkable jobs needing to be done, and versatility by run-time plan . In NoCs, data are managed as packages, while on-chip taking care of parts (PEs) are considered as framework centre points

between related by methods for switches and switches. NoCs give a versatile assumption and huge resource overheads. The NoC layering model parts the trade into four layers:

1) application
2) transport
3) framework; and
4) physical layers.

A crossbar is the basic structure square of the NoC physical layer. A crossbar switch is a typical correspondence medium getting a various passage method to enable physical group exchange. The crucial resource sharing Network grasped by existing NoC crossbars are time-division different access (TDMA), where the physical association is time shared between the interconnected PEs, and space-division multiple access (SDMA), where a submitted association is developed between each match of interconnected PEs. The physical layer of a NoC switch in like manner contains buffering and limit contraptions.

Over-trouble CDMA is a remarkable medium access strategy passed on in distant exchanges where the number of customers sharing the correspondence channel is helped by growing the amount of usable spreading codes to the disservice of extending various passage deterrents (MAI). The over-trouble CDMA thought can be associated with on-chip interconnects to assemble as far as possible

II LITERATURE SURVEY

Intra-chip correspondence is a critical bottleneck in present-day multiprocessor structure on-chip (MPSoC) plots. The vehicle geography is the most notable on-chip interconnect advancement and transport struggle in one of the noteworthy issues in transport based MPSoC plans. Code division multiple access (CDMA) has been proposed as a vehicle sharing framework to overcome the vehicle strife issue. In CDMA, a foreordained number of balanced spreading codes can share the medium due to the Multiple Access Interference (MAI) issue. In far off exchanges, over-trouble CDMA has been considered to grow as far as possible by including extra non-even spreading codes with specific characteristics. We propose a novel CDMA transport configuration using the over-trouble CDMA thoughts to extend the most extraordinary number of focuses having the equivalent CDMA transport in MPSoC by 25% at an immaterial Improved Overloaded CDMA Interconnect (OCI) Bus Architecture for On-Chip Communication.

On-chip interconnect is a vital structure square and a standard execution bottleneck in current complex System-on-Chips (SoCs). The vehicle geography and its auxiliaries are the most sent correspondence structures in contemporary SoCs. Space trading exemplified by crossbars and multiplexers, and time-sharing are the key enabling impacts of various vehicle structures. Our work hopes to enhance the customary CDMA transport incorporates by applying over-trouble CDMA practices to extend the vehicle utilization adequacy. We propose the Difference-Overloaded CDMA Interconnect (D-OCI) transport that utilization the changing Parallel over-trouble CDMA interconnect (OCI) transport building for on-chip trades On-chip interconnects are the execution bottleneck in present-day System-on-Chips (SoCs).

Transport geographies and Networks-on-Chip (NoCs) are the crucial approaches used to realize on-chip correspondence. The interconnect surface enables resource sharing by Time or conceivably Space Division Multiple Access (T/SDMA) techniques. Code Division Multiple Access (CDMA) has been proposed to enable

resource participating in on-chip interconnects where each datum bit is spread by an exceptional balanced spreading code of length N. Not in any manner like T/SDMA, in far off CDMA, the correspondence channel breaking point can be extended by vanquishing the Multiple Access Interference (MAI) issue.

Using OCI in CDMA-based NoCs has the capacity of giving higher exchange speed at low-force and-domain overheads that appeared differently in relation to other NOC structures. Moreover, settled inertness and obvious execution achieved by the basic CDMA synchronization can diminish the effort and overhead required to complete QoS. In this work, we advance the Overloaded CDMA interconnect for Network on- Chip.

III EXIXTING METHODS

In many applications, radiation-induced multiple-cell upsets (MCUs) that can cause soft errors have become a severe concern for memory operation [1]–[4]. To tolerate these errors, error correction codes (ECCs) have been proposed to protect memories at the system level. When only a single bit error occurs in a word, Hamming codes [as a class of single error-correction (SEC) codes] can be utilized to tolerate this bit upset [5]. Although Hamming codes can be improved and even extended to tolerate double and triple adjacent errors in a word [6], [7], complex ECCs with high tolerant function capabilities should be employed in the case of an MCU of larger cardinality [8], [9].

The main drawback of these codes is that they require very complex periphery circuits (encoder and decoder) to implement error detection and correction. simplify the structure of the MLGs; the MLGs are implemented by dividing a γ -input SN into two γ /2-input SNs, so reducing the hardware overheads. However, a considerable number of two-input gates are still required for the majority voting function.

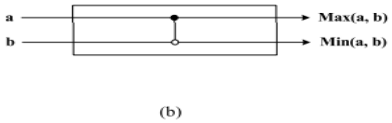


Figure: Two-input SN

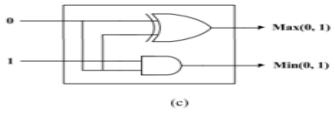


Figure Two-input SN schematic diagram

In this project, a novel design of an MLG is proposed; this MLG consists of two networks (pull-up and pull-down) as well as an inverter. In the proposed design, the pull-up and pull-down networks (for an odd γ , they are mirror circuits) through the inverter generate as output the majority value for an MLG with γ inputs. The application of the proposed MLGs to the design of a fast decoder for OS-MLD codes is also presented. As expected also for this application (and for different codes), the proposed designs are substantially better than existing MLGs. This project is organized as follows.

A. Majority Logic Gate

In one-step ML decoders (such as in Fig. 1), MLGs can correct an erroneous bit on the basis of the majority value of the γ parity-check sums. This is a significant feature because it affects the hardware design and simplifies the complexity of the one-step ML decoder. The function of the MLG includes two cases: when the majority of the inputs are 1, then the majority value is 1; else, the majority value is 0. The majoritythreshold of an MLG is given by γ /2 + 1; however, a specific case occurs when γ is even and the number of zero-valued inputs is the same as the number of one-valued inputs although this is a rather simple technique, the complexity of the MLG circuit

dramatically increases when the number of inputs γ increases.

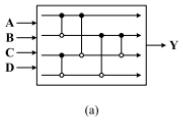
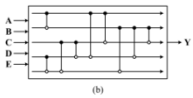


Figure: Four-input MLG (Sort 41)



Five-input MLG (Sort 51)

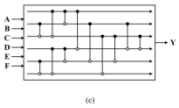
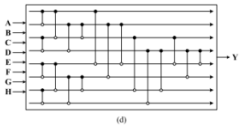


Figure: Six-input MLG (Sort71)



Eight-input MLG (Sort81)

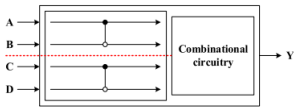


Figure: Four-input MLG based on SN

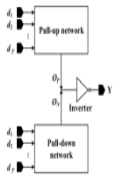


Figure Block diagram of the proposed γ -input MLG

Divide-and-conquer approach; a γ -input SN is divided into two γ /2-input SNs. For example, the four-input MLG of [16] [Fig. 3(a)] is improved by using the scheme of [11] (Fig. 4). The hardware complexity of the MLG is reduced; only seven two-input gates (42 transistors) are needed now (i.e., a 46.2% reduction), and the logic depth of the SN has also been shortened from 6 to 4 (so, a 33.3% reduction). Figures of merit (such as circuit area, power, and delay) are improved. However, this approach still requires a substantial number of transistors to implement an MLG. In some applications such as memories protected by MLD codes, MLGs are the main component of the decoder so the complexity of an MLG has a significant impact on the overall design in terms of area, delay, and power dissipation of this circuit as well as the overheads of the entire memory system. Therefore, there is a need to propose efficient MLG designs at lower complexity than currently found in the technical literature.

Existed Majority Logic Gate

In this section, a new MLG scheme as a low overhead design is proposed and some examples are shown to illustrate in detail the proposed scheme

A. MLG Design

The proposed circuit for the MLG is shown in Fig. 5; it consists of three parts: a pull-up network, a pull-down network, and one inverter. The function of the pull-up network is to output logic 1; similarly, the function of the pull-down network is to output logic 0. Finally, the inverter changes the output of the pull-up or pull-down network from 1 to 0 or from 0 to 1. Consider initially the following definitions/notation. 1) As discussed previously, when the number of inputs γ is even, the majority threshold is given by γ /2 + 1, and at least γ /2 + 1(γ /2) inputs of value 1 (0) can generate a majority of 1 (0). This implies that there are at least Cγ /2+1 γ (Cγ /2 γ) input combinations to generate the majority value of 1 (0) over the exhaustive 2γ combinations. Therefore, the pull-up network is the sum (binary OR operation) over Cγ /2 γ γ /2-input ANDs, and similarly, the pull-down network is the sum over Cγ /2+1 γ (γ /2 + 1)-input ANDs. 2) When the number of inputs γ is odd, the majority threshold is given by (γ + 1)/2. There are at least C(γ +1)/2 γ combinations to generate both majority values (1 and 0) among the 2γ exhaustive input combinations, so both the pull-up and pull-down networks are given by the sum over C(γ +1)/2 γ (γ +1)/2-input ANDs. Table II summarizes the

parameters of the proposed scheme under the two different cases in the number of inputs. 3) Only pMOS (nMOS) transistors are utilized to construct the pull-up (pull-down) network; in these two networks, the AND (OR) operation is implemented by using transistors in series (parallel). 4) As a Boolean function, hereafter the "+" symbol denotes the binary OR operation.

In this section, overloaded CDMA in wireless communications and the requirements of its on-chip interconnect counterpart and preliminaries of the classical on-chip CDMA switch presented by Nikolaet al. [16] are present.

Overloaded CDMA in Wireless Communications

A unique spreading code is assigned to every TX-RX pair sharing the communication channel. Data streams of users sharing the channel are spread and simultaneously transmitted to an additive communication channel. Dispreading is achieved by applying the correlation operation to the received sum, where each receiver can extract its data by correlating it with the assigned spreading code. In wireless communications, random effects such as noise, fading, and multipath arising in the communication channel affect proper identification of the received sum, which increases the bit error rate (BER) of the received data.

Unfortunately, the number of orthogonal codes in a spreading code set is usually limited to the spreading code length N, which reduces the channel utilization efficiency.

In this project, we apply the overloaded CDMA concepts developed in the wireless communication field to on-chip interconnects to increase the CDMA-based NoC capacity. However, on-chip interconnects are significantly different from

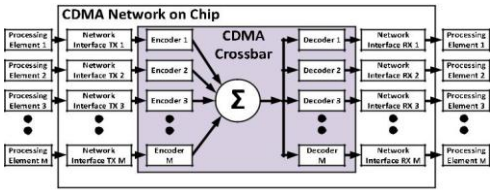


Figure: CDMA NoC router architecture

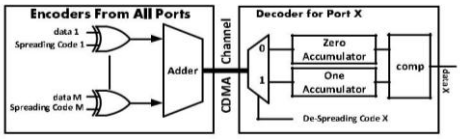


Figure: Classical CDMA crossbar

Wireless communication channels on both the characteristic and requirement levels. In the following, basic features of overloaded CDMA will be enumerated from the on-chip inter-connect perspective to sum up the OCI design considerations.

1) Overloaded CDMA is a medium access technique deployed in wireless communications based on DSSS-CDMA.
2) The complexity of wireless overloaded CDMA limits its applicability for on-chip interconnects, which require simple communication schemes to meet the performance requirements.
3) Despite that wireless CDMA is usually adopted in conjunction with other modulation techniques, only baseband binary CDMA is considered for on-chip interconnects, which can be directly implemented in digital platforms such as FPGAs.
4) Because only digital on-chip interconnects are considered, random effects arising in analog communication channels such as noise, fading, and MAI can be efficiently mitigated using error detection and correction techniques [27]. Therefore, such random effects are neglected in this project.

5) Consequently, due to the last two assumptions, the complexity of the CDMA receivers can be significantly reduced to fit the on-chip interconnect requirements.

Classical CDMA Crossbar Switch

Figureillustrates the high-level architecture of a CDMA-based NoC router. The physical layer of the router is based on the classical CDMA switch presented by Nikolicet al. [16] and illustrated in Fig. 1(b). The switch is composed of a number of XOR encoders, a channel adder, and accumulator-based decoders. In the encoder, an N-chip length binary orthogonal code, generated from a Walsh spreading code set, is XORed with the transmitted data bit and sent out serially, indicating that a single bit is spread in a duration of n clock cycles. Therefore, the crossbar transaction frequency ft and operating clock frequency fc are related as ft= fc/ N.

The data are spread into N chips, where N is the CDMA code length that equals the number of clock cycles in a single crossbar transaction. Spread data chips from all encoders are summed by the CDMA crossbar adder and the sum is sent out serially to all decoders. The encoding/decoding process lasts for N clock cycles synchronized via a counter. At each decoder, the assigned code is cross correlated with the received sum to decode the data from the summed chips. The decoded flits are stored in the receive NI FIFOs until they are read by the PEs. In this project, we focus on the high-level architecture and implementation details of the overloaded CDMA crossbar represented by the grey block.

A store and forward flow control and a deterministic routing algorithm are employed in the OCI router. The routing algorithm lies at the network layer, which is a higher layer than the physical layer containing the crossbar switch. According to the OSI model design principles, each layer of the model exists as an independent layer. Theoretically, one can substitute one protocol for another at any given layer without affecting the operation of layers above or below. Thus, using the same flow control protocol and routing algorithm enables comparing the OCI-based router with SDMA- and TDMA-based routers

A controller block is used for code assignment and arbitration tasks. Each PE is interfaced to an encoder/decoder wrapper enabling data spreading/de-spreading. Unlike orthogonal spreading codes, which are XORed with the binary data bit, an AND gate is utilized to spread data using nonorthogonal spreading codes. The AND gate encoder works as follows: if the transmitted data bit is “0,” it sends a stream of zeros during the whole spreading cycle, which does not cause MAI on the channel; if the transmitted data bit is “1,” the encoder sends a nonorthogonal spreading code.

A. Crossbar Adder

For a spreading code set of lengthN, the number of crossbar TX-RX ports is equal to M=2(N−1). In the T-OCI crossbar, sending a “1” chip to the adder is mutually exclusive between nonorthogonal transmit ports according to the T-OCI encoding scheme. This indicates that among the 2(N−1) inputs to the adder, there are guaranteed (N− 2) zeros, while the maximum number of “1” chips is N. Therefore, a multiplexer is instantiated to select only a single input of the nonorthogonal TDMA encoded data bits and discard the remaining bits that are guaranteed to be “0.” Thus, the adder has only N-bit inputs, N− 1 from orthogonal encoders, and 1 from the multiplexer, as shown in Fig. (d). The sum produced by the adder circuit needs (log2N) wires. The number of needed stages of registers to pipeline the adder is (log2N), as depicted in

Error! Reference source not found.(d). N replicas of the crossbar adder are instantiated for the parallel encoding adopted in the P-OCI crossbar.

B. Custom Decoder

There are four decoder types for different CDMA decoding techniques: the orthogonal T-OCI and P-OCI decoders and the over-loaded T-OCI and P-OCI decoders. The orthogonal T-OCI decoder is an accumulator implementation of the correlator receiver. N− 1 accumulator decoders are instantiated in all CDMA crossbar types for orthogonal data dispreading. Instead of implementing two different accumulators (the zero and one accumulator), an up–down accumulator is implemented and the accumulated result is the difference between the two accumulators of the conventional CDMA decoder. The accumulator adds or subtracts the crossbar sum values according to the dispreading code chip and resets every N number of cycles. The sign bit of the accumulated value directly indicates the decoded data bit, where the positive sign is decoded as "1," while the negative sign is decoded as "0." The P-OCI orthogonal decode (e) differs from the T-OCI orthogonal decoder in receiving the adder sum values concurrently not sequentially; therefore, the accumulator loop is unrolled into a parallel adder.

The P-OCI crossbar bandwidth, however, is the highest of the three crossbars. The T-OCI crossbar bandwidth is double that of the conventional CDMA crossbar because the number of interconnected ports is doubled, while the P-OCI bandwidth is N× 100% higher than that of the T-OCI crossbar. Therefore, the P-OCI crossbar has the highest bandwidth at the expense of higher complexity, while the conventional CDMA crossbar has the lowest bandwidth and complexity and the T-OCI crossbar seizes the middle ground in terms of area and bandwidth.

OCI Crossbar Evaluation

In this section, a comparison among the conventional CDMA, T-OCI, and the P-OCI crossbars is drawn. A crossbar containing a number of TX-RX ports is built with full capacity, i.e., the number of ports is the maximum number offered by the crossbar. All CDMA crossbar architectures in both the reference and pipelined variants are implemented and validated on an Artix-7 AC701 evaluation kit. The developed crossbars are evaluated for different spreading code lengths N = {8,16,32,64}. To establish a fair comparison among different crossbar architectures with different numbers of ports, all utilization metrics are normalized to the number of crossbar ports M. The evaluation results, including the resource utilization expressed in the number of lookup tables (LUTs) and FFs per port, maximum crossbar frequency, dynamic power consumption per port, and crossbar bandwidth, are illustrated.

As depicted, for a spreading code of length N, the resource utilization per port of the T-OCI crossbar is lower than that of the ordinary CDMA crossbar by 31%. This salient reduction in the normalized resource utilization is due to the significant increase in the CDMA interconnect capacity compared with the marginal overhead added by the crossbar circuitry. On the other hand, the P-OCI crossbar is 400% larger than the conventional CDMA crossbar due to the parallel crossbar adders. Increasing the spreading code length N increases the resource utilization per port, due to the increasing crossbar complexity. Specifically, with increasing N, the size of the crossbar adder and accumulator decoder circuitry increases. The resource utilization of all crossbar pipelined variants is always larger than that of the basic architectures due to the additional non architectural pipelining registers.

OCI Communication Reliability Considerations:

Since the OCI scheme relies on adding detectable interference to the interconnect, the robustness of the OCI crossbar to noise may be raised as a concern; would the added MAI reduce the robustness of the OCI compared with that of the conventional CDMA interconnect? According to [27], while full-swing digital implementations have typically been able to assume BER values less than 10−15 over the operating range of voltages and frequencies, this assumption does not hold true for custom low-swing interconnect implementations and modern deep sub micrometre circuits.

Indeed, in wireless communication channels, overloaded CDMA would increase the BER compared with the classical CDMA because of overloading the channel with MAI. The binary nature of the OCI interconnect enables enhancing its robustness by employing error detection and correction techniques to mitigate such random effects.

To empirically test the robustness of the OCI crossbar on the FPGA platforms, a test bench was applied for N= 16 OCI crossbar implemented on a Zed board FPGA evaluation kit with a 100-MHz clock frequency and a 1 V core voltage. Zynq's embedded processor runs a program generating 106 consecutive crossbar transactions and compares the decoded output with the input data. Zero errors were detected during the experiment, which lasted for 27 h.

OCI for NoCs: Analytical Evaluation

An analytical comparison between the OCI crossbars and some existing bus and NoC interconnection techniques. The comparison is established for an interconnect

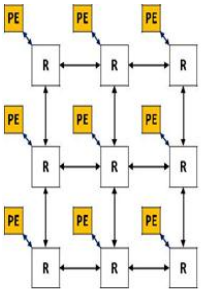


Figure: CONNECT torus topology

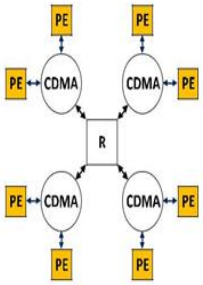


Figure: OCI star topology

The OCI technique can be applied to the peripheral bus to increase the number of interconnected PEs and peripherals without degrading the transaction latency. In the CDMA parallel transfer wrapper of [17] and [18], the number of parallel transfer lines is reduced by bundling data using spreading codes. The OCI spreading codes can be therefore, the OCI crossbar can provide higher bandwidth than the CDMA peripheral bus and the CDMA parallel transfer wrapper of the same complexity due to crossbar overloading.

The CDMA encoding–decoding scheme presented in [25] is based on the standard basis TDMA codes, which replace the orthogonal Walsh codes. The encoders are consequently replaced by an AND gate, the bus adder is reduced to a single XOR gate, the channel wires are reduced to one wire per bit because no two TDMA chips are simultaneously sent in the same clock cycle. This scheme resembles TDMA signalling but adopts the CDMA arbitration procedures where the code assignment is done once every N encoding–decoding bus cycle. On the other hand, our proposed OCI technique enables coexistence between both CDMA and TDMA codes on a single channel, providing double bandwidth, while utilizing less area than two independent TDMA and CDMA crossbars.

New CDMA Encoding & Decoding Method

The basic structure of applying CDMA technique to NoC with a star topology is shown in Fig. 1. In this figure, a PE executes tasks of the application and network interface (NI) divides data flows from PE into packets and reconstruct data flows by using packets from NoC. Each node needs two chip counters, one for the sender and the other for the receiver. Note that packet flits from NI can also be transformed to multiple bit streams in the P2S module to make trade-offs between power/area cost and packet transfer latency, and the scheduler should provide a bit-synchronous scheme to maintain the orthogonality of the transmitted channels, as discussed in [8]. In this brief, we focus on the design and comparison of WB- and SB-based CDMA encoding/decoding method, which corresponds to E, A, and D modules.

CDMA Encoder

Two different encoding methods, WB encoder and SB encoder.

An original data bit is first encoded with a Walsh code by taking an XOR operation. Then, these encoded data are added up to a multibit sum signal by taking arithmetical additions. Each sender needs an XOR gate, and multiple wires are used to express the sum signal if we have two or more senders. Therefore, the output signal is always a sequence of binary signal transferred to destination using one single wire. The progressions of both the encoding schemes are depicted the WB encoding process with four-chip Walsh codes and the SB encoding process with four-chip standard orthogonal codes, respectively

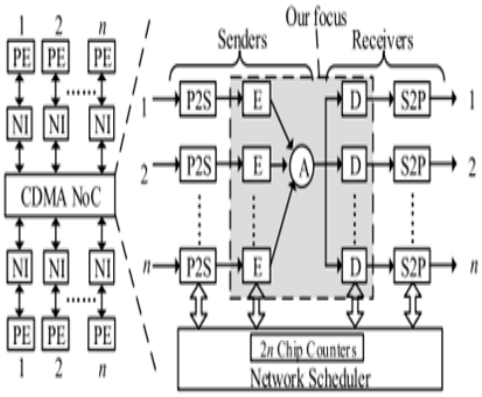


Figure: Structure of CDMA NoC

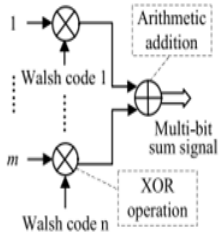


Figure: Block Diagram of Encoding Scheme - WB Encoder

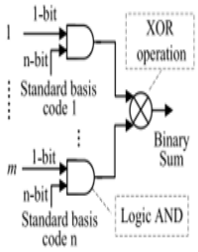


Figure: Block Diagram of Encoding Scheme - SB Encoder

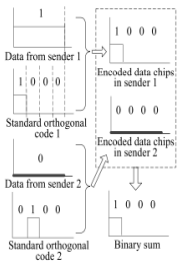


Figure: Data Encoding Example - WB Encoding

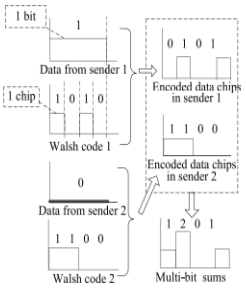


Figure: Data Encoding Example - SB Encoding

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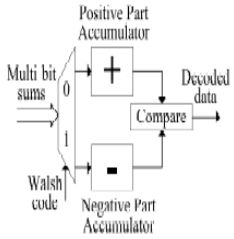

Figure Block Diagram Of Decoding Scheme - WB Encoder

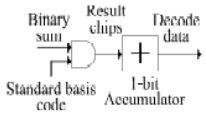

Figure: Block Diagram Of Decoding Scheme - SB Encoder

CDMA Decoder

According to the chip value of Walsh code, the received multibit sums are accumulated into positive part (if the chip value is 0) or negative part (if the chip value is 1). Therefore, the two accumulators in the WB decoder separately contain a multibit adder to accumulate the coming chips and a group of registers to hold the accumulated value. Through the comparison module after the two accumulators, the original data is reconstructed. If the value of positive part is large, the original data is 1.

the WB decoder of receiver 1, the accumulated value 3 in the positive part is larger than the accumulated value 1 in the negative part. By the WB decoding scheme, the decoded data is 1, which is equal to the source data bit from sender 1. In Fig. 5(b), at the SB decoder of receiver 1, the output value of the accumulator is 1, which is also equal to the source data bit from sender 1. Note that the decoding results in receiver 2 are also correct but are not shown in the figure. Hence, both methods can reconstruct the original data bit from the sum signal by using their respective spreading codes.

Data Encoding Example:

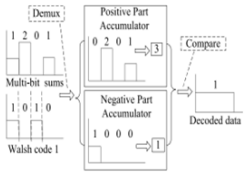

Figure: WB Decoding at Receiver 1

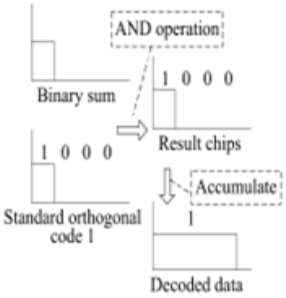

Figure SB Decoding at Receiver 1

IV SIMULATION RESULTS

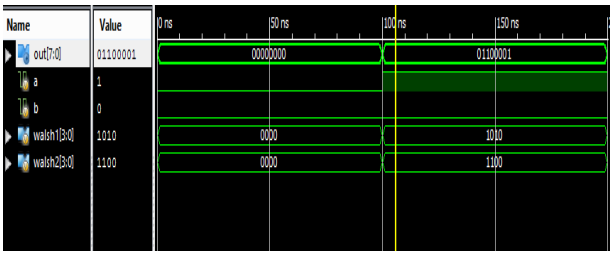

Figure1: WB Encoder

From fig.1 and fig.2The encoded information from two senders are combined through xor activity, and a paired aggregate sign is generated. Therefore, the yield signal is consistently a succession of double sign moved to goal utilizing one single wire. The movement of both the encoding plans are delineated from fig.1. what's more, fig.2. In WB disentangling scheme the chip estimation of walsh code, the got multi bit entireties are amassed positive part or negative part by utilizing comparator we need to think about positive and negative parts, if positive is more prominent than negative then the first information is 1, in any case the first information is 0.

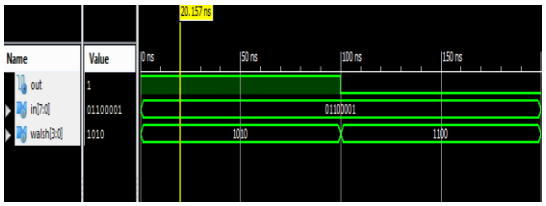

Figure: WB Decoder

From fig.3 and fig.4 in SB encoding plan unique information bit from a sender is taken care of into an AND door in chip by chip way and encoded information from an alternate senders are combined by a XOR activity and a double total sign is created. In SB translating schema the parallel whole sign shows up at recevers,an AND activity is taken between double aggregate and relating entirety then the outcome is sent to a collector the yield of the gatherer will be the comparing unique information.

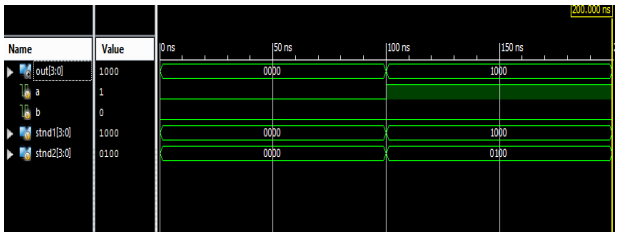

Figure: SB Encoder

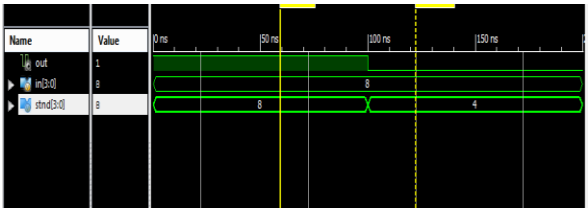

Figure: SB Decoder

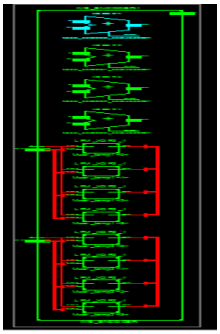

Figure: RTL schematic

Design Summary:

Device Utilisation Summary (Estimated Values)

Logic Utilization	Used	Available	Utilization
Number of Slices	4	5888	0%
Number of 4 input LUTs	8	11776	0%
Number of bonded IOBs	18	372	4%

Estimated Values

Timing Constraints

```
Timing constraint: Default path analysis
  Total number of paths / destination ports: 32 / 8
-------------------------------------------------------------------------
Delay:               7.337ns (Levels of Logic = 3)
  Source:            b (PAD)
  Destination:       out<6> (PAD)

  Data Path: b to out<6>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             8   0.849   0.900  b_IBUF (b_IBUF)
     LUT4:I0->O            1   0.648   0.420  out<6>1 (out_6_OBUF)
     OBUF:I->O                 4.520          out_6_OBUF (out<6>)
    ----------------------------------------
    Total                      7.337ns (6.017ns logic, 1.320ns route)
                               (82.0% logic, 18.0% route)
```

Figure Timing Constraints

V CONCLUSION

In this Project, we introduced the concept of overloaded CDMA crossbars as the physical layer enabler of NoC routers. In overloaded CDMA, the communication channel is overloaded with non-orthogonal codes to increase the channel capacity. Two crossbar architectures that leverage the overloaded CDMA concept, namely, T-OCI and P-OCI, are advanced to increase the CDMA crossbar capacity by 100% and 2N× 100%, respectively, where N is the spreading code length. We exploited featured properties of the Walsh

spread-ing code family employed in the classical CDMA crossbar to increase the number of router ports sharing the crossbar without altering the simple accumulator decoder architecture of the conventional CDMA crossbar. Generation procedures of nonorthogonal spreading codes are presented along with the reference and pipelined architectures for each crossbar variant. The T-/P-OCI crossbars were implemented. The performance of the OCI crossbars is compared with that of the conventional CDMA crossbar. The dynamic power is reduced by 45% for the T-OCI crossbar but increased by 133% for the P-OCI crossbar. The T-OCI crossbar utilizes 31% fewer resources, while the P-OCI crossbar uses 400% more resources compared with the conventional CDMA crossbar. The OCI crossbar suitability for NoCs has been established by analytically and experimentally evaluating a fully working OCI-based NoC. A 65-node OCI-based star NoC was realized and compared with an SDMA-based torus NoC generated by CONNECT. The evaluation results demonstrate the superiority of the OCI-based NoCs in terms of area and throughput.

Applications and advantages:

- It contains bigger limit
- GSM band width =200khz
- Easy to expansion more clients
- Better transmission information contrast with TDMA/FDMA

VI FUTURE SCOPE

Many future work directions are inspired by this project including exploiting the mathematical properties of the code space to find additional nonorthogonal codes and boost the CDMA interconnect capacity and exploring more architectural optimizations of the OCI crossbar. Studying the robustness of CDMA interconnects and its enhancement techniques will be one of the prior future research points. Moreover, we plan to investigate using the OCI-based routers in different network topologies, evaluate their performance using standard benchmarks, and study their suitability for various applications.

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