|| Volume 5 || Issue 11 || November 2020 || ISSN (Online) 2456-0774
INTERNATIONAL JOURNAL OF ADVANCE SCIENTIFIC RESEARCH
AND ENGINEERING TRENDS

AN ENERGY EFFICIENT HIGH SPEED ECRL BASED FULL ADDER DESIGN

[1]Jillella Mounika,[2] Maddi Hemalatha

[1]M.Tech PG Scholar,[2] Assistant Professor, M. Tech[Ph.D.]
[1,2] Department OF E.C.E.
[1,2]Chadalawada Ramanamma Engineering College, Tirupati, Andhra Pradesh, India

---

Abstract:- In this paper an improved structure for efficient charge recovery logic is presented. In order to optimize the power dissipation of digital systems, high speed analysis should be applied throughout the design process from system level to process level. We proposed ECRL logic is a very low power design that dissipates less amount of power. The ECRL adiabatic technique is mainly used for reducing the power dissipation in VLSI circuits by performing charging and discharging process. The full adder plays an important role in many arithmetic operations such as the adder, multiplier and divider and processors. In order to limit the power dissipation, an energy efficient high-speed ECRL full adder is designed in this paper. The Full Adder circuit designed with low power ECRL adiabatic technique is compared with 1-bit conventional Full Adder circuit using domino logic and the simulation results are obtained using Tanner EDA tool.

Keywords: *Adiabatic logic, ECRL, Low Power Dissipation, Delay, FullAdder*

I INTRODUCTION

In today's era, power dissipation is the main issue for designing the VLSI circuits. By using various technologies, we can design our circuit by considering the constraints which cannot be neglected. In Very Large-Scale Integration Circuit, performance plays a vital role for the architecture of low power and high speed in the circuit.To achieve higher performance of the CMOS device circuit along with high densities, there have been reductions in supply voltages, device dimensions, and transistor threshold voltages over the years. But these reductions have also resulted in higher leakage currents that can severely affect power consumption in a circuit. The power consumption of any CMOS VLSI circuit is made up of dynamic energy and static energy. Dynamic power dissipation is due to circuit switching activities, while static power dissipation occurs due to leakage components of the circuit during standby mode. During submicron technology, when the size of the function was greater than 350 nm, the leakage power dissipation was less than the dynamic power by several orders of magnitude [1]. With technology scaling, it is necessary to reduce the supply voltage and threshold voltage of VLSI circuits. However, lowering the threshold voltage increases static power dissipation. In ultra-deep submicron technology, where the function size is less than 100nm, the static power dissipation has dominated the dynamic power. Therefore, there is a need to reduce static power dissipation in ultra-deep submicron technology.

In VLSI, Domino Logic is the most prominent technique which is used to reduce the power. In Very Large-Scale Integration Circuit, performance plays a vital role for the architecture of low power and high speed in the circuit. Domino Logic has proven to be a useful circuit in VLSI technology. Domino logic has various advantages like small space and highspeed operation compared to its fixed CMOS counterparts [2]. It uses the best characteristic of static and dynamic logic without suffering from the sensitivity of the load capacity as it does in pure dynamic logic [3]. Domino logic is a logical family registered which means there is a clock in every logic gate. The continuous clock switching in domino logic design increases the power dissipation. Several techniques have been proposed to reduce power dissipation in the domino logic unit such as scaling the supply voltage [4] or using a low swing clock [5] but little focus has been placed on the clock gate technology [6] that uses a clock enable circuit has been used.

Adiabatic Logic is another most prominent technique which plays a very vital role for the power consumption in the circuit. Adiabatic logic aims to decrease the power in the logic circuit. In digital circuits the power dissipation can be reduced by using several adiabatic logics. Adiabatic

circuits use 'Reversible logic' to conserve energy. It works with the concept of switching activities which reduces the power, by giving the stored energy back to the supply, so that the power dissipation is reduced.

Adders are the basic building blocks of any circuit that are designed to perform high speed arithmetic operation. And they are the most significant logic modules used in digital VLSI circuits. It performs the operations such as multiplying, logical operations, increment and decrement, counting and shifting etc. In amount to carrying out the responsibilities of addition, the adder precedes the source for many difficult circuits like the multipliers, subtractors, RAMs, report calculations and much more.

In this paper, a full adder is designed by using ECRL adiabatic logic and it is compared with the existing 1-bit conventional full adder using domino logic.

II.EXISTING METHOD

A standard domino logic module consists of a pull-down network (PDN), dynamically connected, followed by a static inverter as shown in Fig.1. The non-inverting output of domino is represented by signal *out* while domino node is represented by *X*. The PDN is built exactly as that in complementary CMOS. The domino module works in two phases – *pre-charge* and *evaluation*, where the signal *clock* controls the mode of operation as shown below:

$$clock = \begin{cases} 0, & \text{precharge phase} \\ 1, & \text{evaluation phase} \end{cases}$$

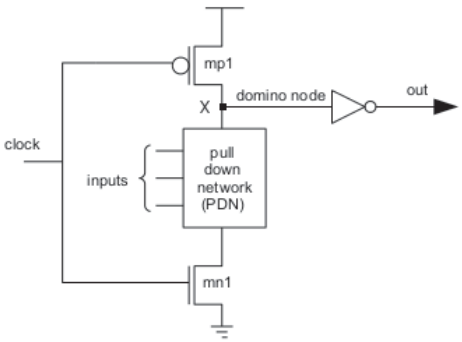

Fig.1. A Standard Domino Logic Module

The existing design of domino logic is shown in Fig.2. The existing uses clock gating in order the pass the clock only during the active state of the circuit. During standby mode, when the inputs of PDN are not changing, clock is not passed to the domino module and the output value of the circuit is hold till the next input transition. Figure shows the proposed design of the domino CMOS logic.

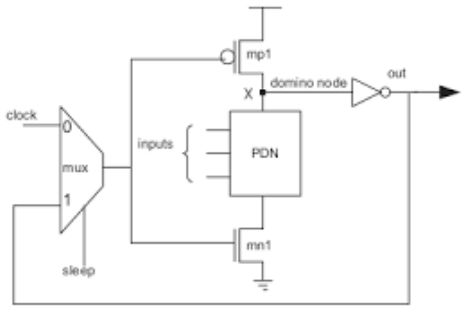

Fig.2. Existing Design for Domino Logic

Here, a 2:1 multiplexer, mux, is used for clock gating and output hold. The multiplexer is designed using transmission gates which combine the complementary properties of NMOS and PMOS transistors. This mux shown in Fig.3. is used for selecting one out of two inputs i.e. clock or out.

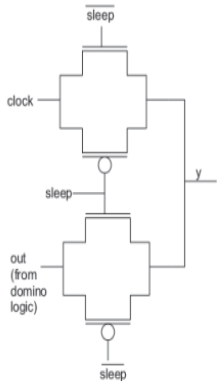

Fig.3. A 2:1 Multiplexer is used in Domino Logic

Signal clock and output are the inputs of mux while y is the output. The sleep is the control signal of mux. The output of mux i.e. signal y is as follows

$$y = \begin{cases} clock, & \text{if } sleep =' 0' \\ output, & \text{if } sleep =' 1' \end{cases}$$

The value of signal sleep is as follow:

$$sleep = \begin{cases} '0' & \text{for active mode} \\ '1' & \text{for standby mode} \end{cases}$$

III.OPERATION OF THE EXISTING DOMINO LOGIC:

When the PDN inputs are changing and the circuit is in active mode, the suspend signal is "0" and y = clock. The clock signal passes to the mp1 and mn1 transistors and operates the standard domino logic functionality. When the inputs do not change, the suspend signal is "1" while y = out. This will maintain the state of the circuit as explained below. Let Out = 1 during standby. This means that the domino node X = 0. Therefore, PDN is in conduction mode. Now, let the dream change from "0" to "1". Therefore, the y signal will change from clock to meaning "1". So mn1 is on while mp1 is off. Since PDN is already in conduction mode, the domino node becomes "0" while the value out = 1 is preserved. The Fig.4. shows the domino logic with the clock synchronized during standby and out = 1. Fig.5. shows the waveform of the proposed design for a 2-input NAND gate for A = '1', B = '1' and the suspend signal changes from '0' to '1'. It can be seen that when the sleep signal becomes '1', out stops oscillating preventing energy dissipation. Let out is "0" during standby. This means X = 1. Therefore, PDN is not conducting. Let the dream change from "0" to "1". Now the values of and will also change from clock to out, which means '0'. The value y = 0 puts mn1 in the off state while mp1 is on. Therefore, X is charged to VDD preserving the state of the circuit. In the proposed design, neither the clock is present in the domino module during standby mode, nor does the output oscillate preventing power dissipation in the circuit.

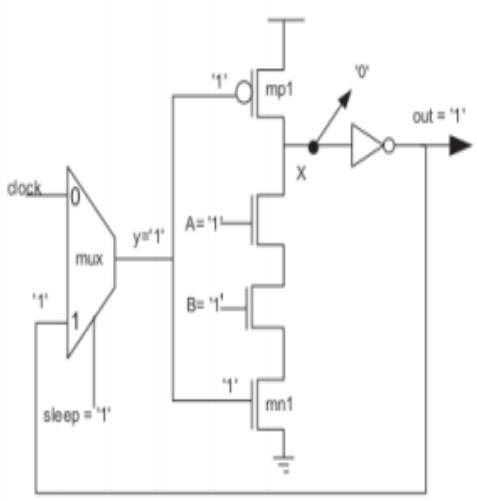

Fig.4.Design for a 2-input nand gate during standby mode without='1'

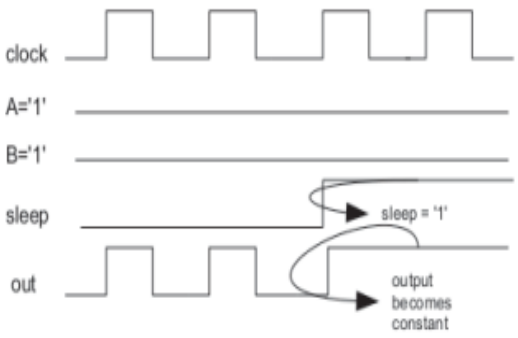

Fig. 3 Waveforms for 2-input nand gate during standby mode

Due to the consumption of minimum area of silicon, the dynamic full adder is faster as well as more compact. It also absorbs not only more power but also more susceptible to the noise in comparison to the static full adder. Fig.6. shows the existing design for a 1-bit conventional full adder using domino logic.

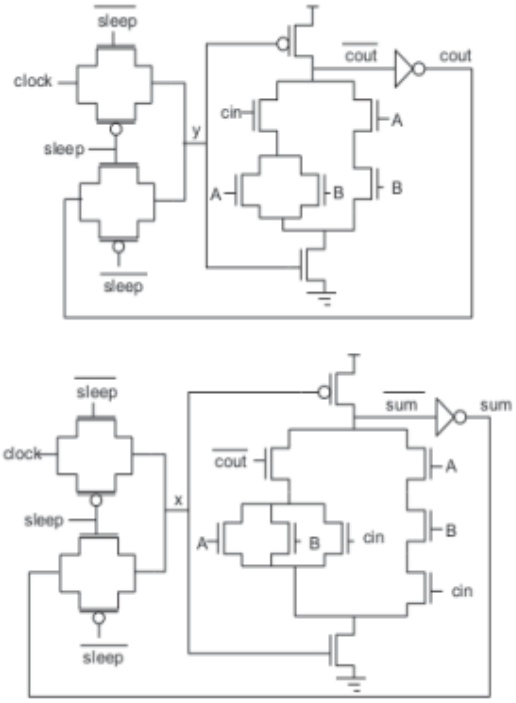

Fig.6. A 1-bit conventional full adder circuit using domino logic

When sleep is low, clock is activated. When clock is low, it is pre-charge phase the pmos with clock signal as input is activated. And hence the since the pmos is on supply is transferred to cout bar. Then output cout bar is

high and cout will be low. And when the clock signal signal is high, it is the evaluation phase. Here actual circuit operation occurs. Since clock is high the pmos transistor with clock as input is off and hence the pmos transistor is off, the supply will not be transferred to cout bar cout bar will be low. Hence cout will be high.

When sleep is low, clock is activated. When clock is low, it is precharge phase the pmos with clock signal as input is activated. And hence the since the pmos is on supply is transferred to sum bar.Then output sum bar is high and sum will be low. And when the clock signal signal is high, it is the evaluation phase. Here actual circuit operation occurs. Since clock is high the pmos transistor with clock as input is off and hence the pmos transistor is off, the supply will not be transferred to sum bar sum bar will be low. Hence sum will be high.

IV.PROPOSED METHOD

Low power circuits aim to provide the best output and use the least amount of energy. The need for low-power VLSI circuits is increasing day by day due to the remarkable success and growth of the category of personal computing devices and wireless communication systems that require high-speed calculations and complex functions with low energy consumption Large energy dissipation requires larger heat sinks thus increasing the space and cost, thus highlighting the need for power circuits Low and important. Adiabatic logic is based on the principle of adiabatic switching. The term "adiabatic" refers to a process in which there is no heat exchange with the environment. The adiabatic switching technology can achieve very low power dissipation, but at the cost of circuit complexity. Adiabatic logic provides a way to reuse the energy stored in the load capacitors instead of the traditional method for discharging the load capacitors to the ground and wasting this energy.

ECRL provides a new method which performs pre-charge and evaluation at the same time where it eliminates the pre-charge diode and dissipates the less energy. Fig.7. shows the basic structure of ECRL. Itconsists of 2 cross-coupled PMOS transistors in the pull up section whereas the pull-down section is constructed with a tree of NMOS transistors. Its structure is similar to the cascade voltage switch logic with differential signaling. The logic function in the functional block can be realized with only NMOS transistors in pull down section.

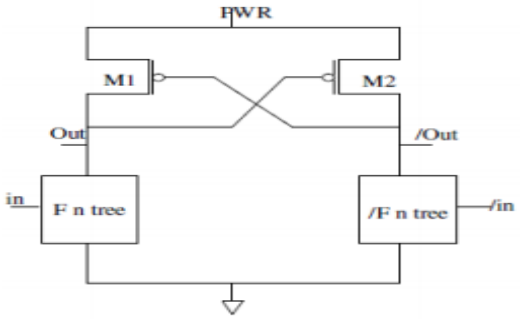

Fig.7. Basic structure of ECRL

ECRL performs pre-charging and evaluation simultaneously where it eliminates pre-charge diode and dissipates less energy. VDD is used to recover and reuse supply power. The schematic diagram of OR/ NOR gate using ECRL is shown in Fig.8. OR/ NOR gate multiplies A and B. It comprises of two outputs such that one output OUT gives the operation of OR gate and outbar gives the complimentary operation of OR gate i.e. NOR gate.

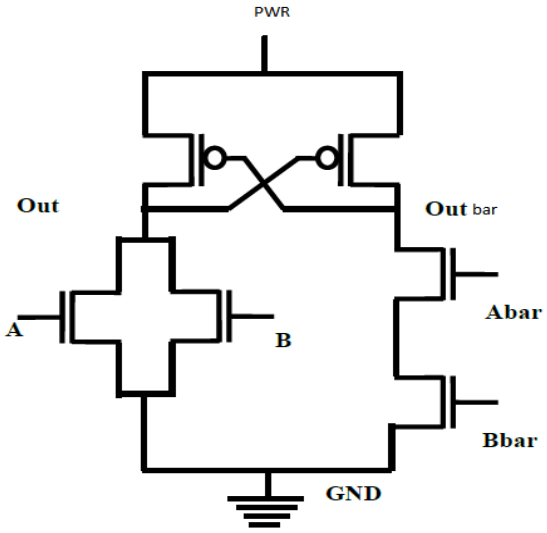

Fig.8. Schematic Diagram of NOR Gate Using ECRL.

Circuit Operation :

Case (i):

When CLK is high, the transistors with input signal A and B are off (since A=0 &B=0) on and the transistors which have inputs Abar and Bbar are on. Since initially out is zero , the P2 transistor is on and hence the output Outbar is high. The voltage at outbar drops to ground since both Abar and B bar are on . Since feedbacks as input to P1, P1 will be on(since outbar=0) and hence out will be high.

Case (ii):

When CLK is high, the transistors with input signal A is off and the transistor with signal B is on (since A=0 &B=1) and the transistors which have inputs Abar is on and Bbar is off. Even though previous out is high , since B is high, it drops to ground. the P2 transistor is on and hence the output Outbar is high. Since feedbacks as input to P1, P1 will be off. and hence out will be low.

Case (iii):

When CLK is high, the transistors with input signal A is on and the transistor with signal B is off (since A=1&B=0) and the transistors which have inputs Abar is on and Bbar is off. since previous out is low , the P2 transistor is on and hence the output Outbar is high. Since feedbacks as input to P1, P1 will be off. and hence out will be low.

Case (iv):

When CLK is high, the transistors with input signal A and B are on(since A=1 &B=1) and the transistors which have inputs Abar and Bbar are off. Initially previous out is low , the P2 transistor is on and hence the output Outbar will be high. Since it feedbacks as input to P1, P1 will be off and hence out will be low.

The schematic diagram of AND / NAND gate using ECRL is shown in Fig.9. AND / NAND gate multiplies A and B. it comprises of two outputs such that one output OUT gives the opera-tion of AND gate and outbar gives the complimentary operation of AND gate i.e. NAND gate.

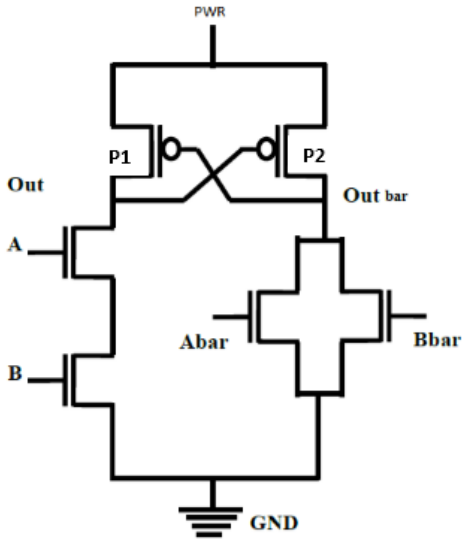

Fig.9. Schematic Diagram of NAND Gate Using ECRL.

Circuit Operation :

Case (i):

When CLK are high, the transistors with input signal A and B are off (since A=0 &B=0) on and the transistors which have inputs Abar and Bbar are on. Since initially out is zero , the P2 transistor is on and hence the output Outbar is high. The voltage at outbar drops to ground since both Abar and B bar are on . Since feedbacks as input to P1, P1 will be on(since outbar=0) and hence out will be high.

Case (ii):

When CLK are high, the transistors with input signal A is off and the transistor with signal B is on (since A=0 &B=1) and the transistors which have inputs Abar is on and Bbar is off. Since previous out is high , the P2 transistor is off and hence the output Outbar is low. Since feedbacks as input to P1, P1 will be on(since outbar=0) and hence out will be high.

Case (iii):

When CLK are high, the transistors with input signal A is on and the transistor with signal B is off (since A=1&B=0) and the transistors which have inputs Abar is off and Bbar is on. Since previous out is high , the P2 transistor is off and hence the output Outbar is low. Since feedbacks as input to P1, P1 will be on(since outbar=0) and hence out will be high

Case (iv):

When CLK are high, the transistors with input signal A and B are on(since A=1 &B=1) and the transistors which have inputs Abar and Bbar are off. Initially previous out is high , the P2 transistor is off and hence the output Outbar is low. Since feedbacks as input to P1, P1 will be on(since outbar=0) and hence out will be low.

By using the proposed ECRL Nand gate, we are designing the full adder circuit. The circuit diagram of ECRLnand gate based full adder is shown in the Fig.10.

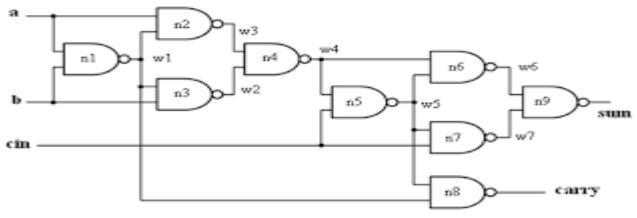

Fig.10. Circuit Diagram of Full adder Gate Using ECRL NAND Gates.

|| Volume 5 || Issue 11 || November 2020 || ISSN (Online) 2456-0774
INTERNATIONAL JOURNAL OF ADVANCE SCIENTIFIC RESEARCH AND ENGINEERING TRENDS

V. RESULTS

The simulation results of ECRL full adder and 1-bit conventional full adder using domino logic circuits have been simulated and discussed in this section. These Simulations are carried out using Tanner EDA tool. The average power consumption of the full adder is analyzed and the comparison is mentioned in Table.1.

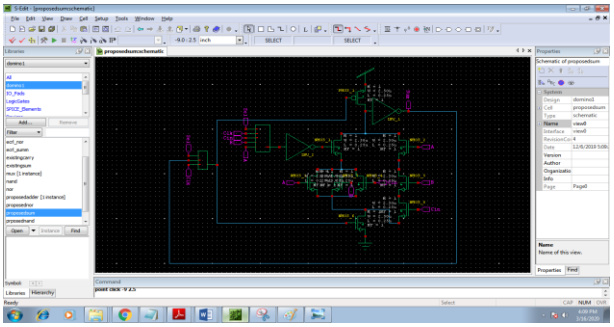

Fig.11. Schematic Diagram of SUM of Full Adder using Domino Logic

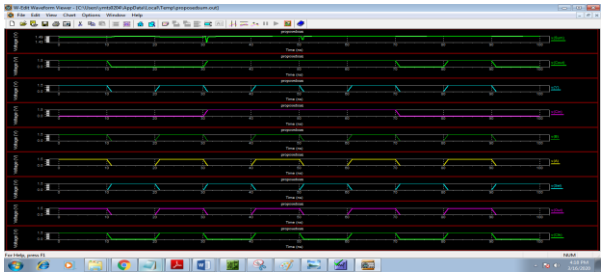

Fig.12. Simulation Results of SUM of Full Adder using Domino Logic

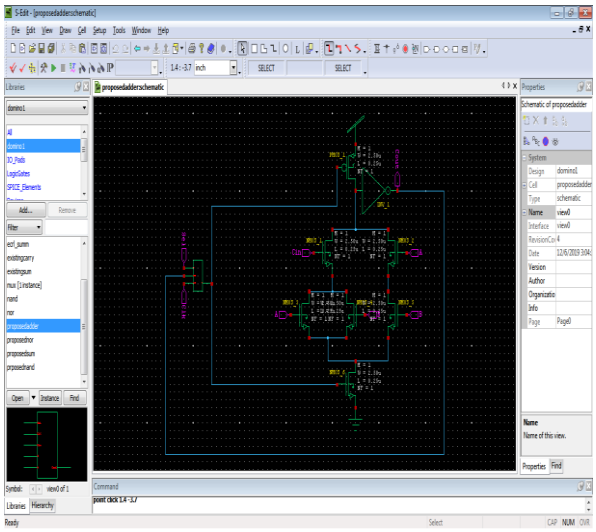

Fig.13. Schematic Diagram of CARRY of Full Adder using Domino Logic

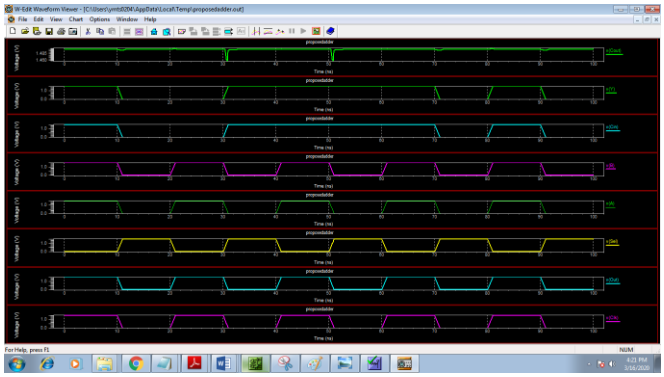

Fig.14. Simulation Results of CARRY of Full Adder using Domino Logic

The Fig.12. and Fig.14. shows the simulated result for 1-bit conventional full adder using domino logic. The input values are based on the truth table of full adder.Based on the operation the obtained average power is 0.6202mw.

The schematic of ECRL full adder is designed using nine ECRL NAND gates.The Fig.16. shows the simulated result for ECRL full adder. Based on the operation the obtained average power is 0.5402mw.

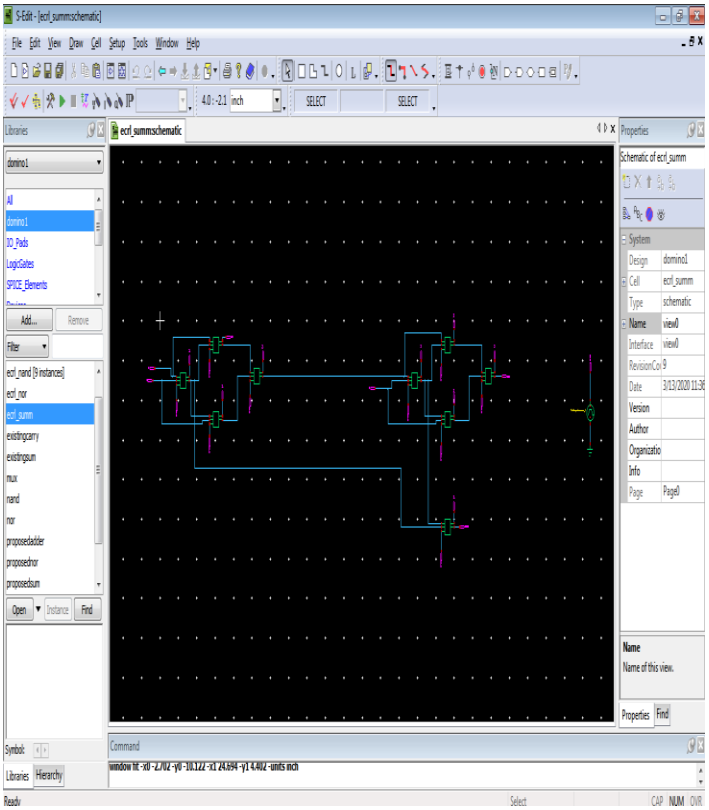

Fig.15. Schematic Diagram of ECRL Full adder Gate Using ECRL NAND Gates.

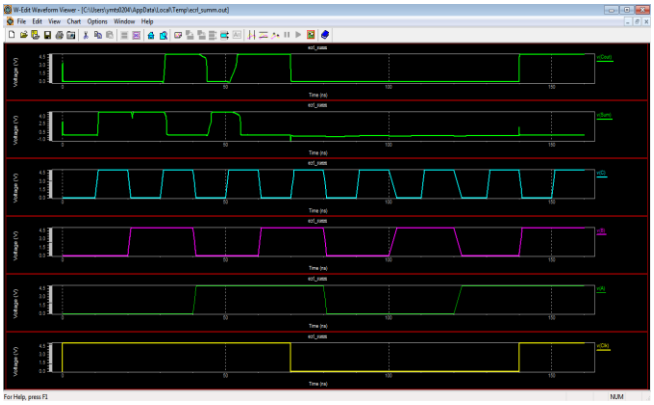

Fig.16. Simulation Results of ECRL Full Adder using ECRL NAND Gates

The ECRL logic gives the better performance in terms of average power dissipation compare with previous technique.The Table.1 compares the analysis of various parameters such as transistor count, average power and delay are calculated by this table.

Table.1 Comparison of ECRL Full Adder and Full Adder using Domino Logic

Parameters	Existing Method	Proposed Method
Power(mw)	0.620	0.540
Delay (ns)	110.24	21.118
Transistor Count	55	90

VI.CONCLUSION

From simulation results it may be observed that proposed ECRL Full Adder circuit offers improved performance with reduced power dissipation and decreased delay. ECRL adiabatic technique is highly helpful for implementation of power efficient designs. This logic is alternative technique for circuit design as compared to pipelining and other techniques that requires high circuit complexity. Energy recovery logics has successfully used for fundamental VLSI blocks such as adder, subtractor and other arithmetic circuits. According to simulations results, delay of proposed ECRL full adder is less than domino logic full adder circuit. Also, the power consumption of proposed ECRL Full Adder has been compared with 1-bit conventional Full Adder circuit using domino logic shows improved performance. Hence it is concluded that the proposed design circuit will provide a platform for designing high performance and low power digital circuits such as digital signal processorsand multiplexers.Hence, this device is suitable for low power devices.

REFERENCES

[1] G. K. Yeap, *Practical low power digital VLSI design*. Springer Science & Business Media, 2012.

[2] S.-Y. Ahn and K. Cho, “Small-swing domino logic based on twist-connected transistors,” *Electronics Letters*, vol. 50, no. 15, pp. 1054–1056, 2014.

[3] J. Pretorius, A. S. Shubat, and C. Salama, “Analysis and design optimization of domino CMOS logic with application to standard cells,” *IEEEjournal of solid-state circuits*, vol. 20, no. 2, pp. 523–530, 1985.

[4] S.-O. Jung, K.-W. Kim, and S.-M. Kang, “Low-swing clock domino logic incorporating dual supply and dual threshold voltages,” in *Proceedingsof the 39th annual Design Automation Conference*. ACM, 2002, pp. 467–472.

[5] M. R. Casu, M. Gelmi, G. Masera, G. Piccinini, and M. Zamboni, “A reduced clock swing domino gate in sol,” in *SOl Conference, IEEEInternational 2002*, 2002, pp. 91–92.

[6] S. Farah and M. Bayoumi, “A comprehensive operand-aware dynamic clock gating scheme for low-power domino logic,” in *SOC Conference(SOCC), 2013 IEEE 26th International*. IEEE, 2013, pp. 349–354.