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FAULT CURRENT CONTROL BY USING DYNAMIC VOLTAGE RESTORER

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***Abstract*—This paper introduces and evaluates an auxiliary control strategy for down stream fault current interruption in a radial distribution line by means of a dynamic voltage restorer (DVR). The proposed controller supplements the voltage-sag reduction control of the DVR. It does not require phase-locked loop and independently controls the magnitude and phase angle of the injected voltage for each phase. Fast least error squares digital filters are used to estimate the magnitude and phase of the measured voltages and effectively reduce the impacts of noise, harmonics, and disturbances on the estimated phas or parameters, and this enables effective fault current interrupting even under arcing fault conditions. The results of the simulation studies performed in the PSCAD/EMTDC software environment indicate that the proposed control scheme: 1)can limit the fault current to less than the nominal load current and restore the point of common coupling voltage within10ms;2)can interrupt the fault current in less than two cycles;3) limits the dc-link voltage ost and, thus, has no restrictions onthedurationoffaultcurrentinterruption;4)performs satisfactorily even under arcing fault conditions; and 5) can interrupt the fault current under low dc-link voltage conditions.**

***Index Terms*—Digital filters, dynamic voltage restorer (DVR), fault current interrupting, multi loop control.**

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I. INTRODUCTION

THE DYNAMIC voltage restorer(DVR)is a custom power device utilized to counter act voltages ags[1],[2].It injects controlled three phase a c voltages in series with the supply voltage, subsequent to a voltages ag, to enhance voltage quality by adjusting the voltage magnitude, wave shape, and phase angle [3]–[6].Fig.1shows the main component so fa DVR(i.e., series transformer T_s, a voltage- source converter (VSC), a harmonic filter, adc side capacitorC_{DC},and an energy storage device [7], [8]). The line-side harmonic filter [5] consists of the leakage inductance of the series transformer L_f and the filter capacitor C_f.

The DVR is conventionally bypassed during a downstream fault to prevent potential adverse impacts on the fault and to protect the DVR components against the fault current[9]–[11]. A technically elaborate approach to more efficient utilization of the DVR is to equipit with additional control sand enable it

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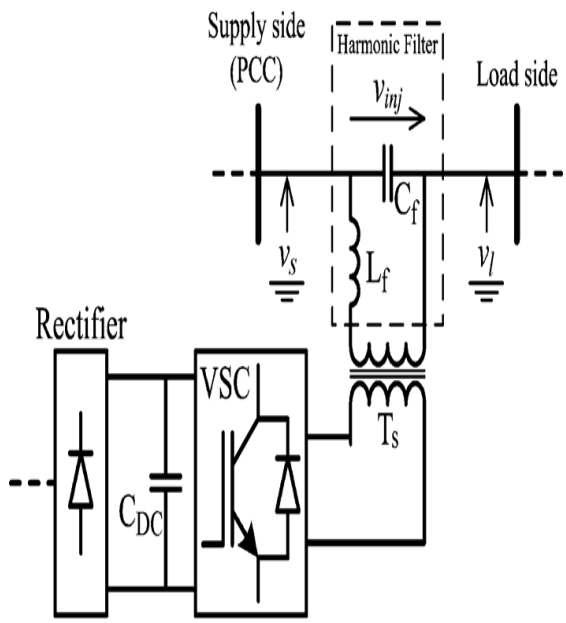

Fig. 1.Schematic diagram of a DVR with a line and load-side harmonic filter.

also to limit or interrupt the downstream fault currents. A control approach to enable a DVR to serve as a fault current limiter is provided in [9]. The main drawback of this approach is that the dc-link voltage of the DVR increase sue to real power absorption during fault current-limiting operation and necessitates a switch to bypass the DVR when the protective relays, depending on the fault conditions, do not rapidly clear the fault. The dc-link voltage increase can be mitigated at the cost of a slow-decaying dc fault current component using the methods introduced in [7] and[12].

To overcome the a fore mentioned limitations, this paper pro poses an augmented control strategy for the DVR that provides:

1) voltage-sag compensation under balanced and unbalanced conditions and

2)a fault current interruption(FCI)function. The former function has been presented in [13] and the latter is described in this paper.

It should be noted that limiting the fault current by the DVR disables the main and the backup protection (e.g., the distance and the over current relays). This can result in prolonging the fault duration. Thus, the DVR is preferred to reduce the fault current to zero and interrupt it and send a trip signal to the up- stream relay or the circuit breaker (CB).

It should be noted that the FCI function requires 100% voltage injection capability. Thus, the power ratings of the series transformer and the VSC would be about three times those of a conventional DVR with about 30%–40% voltage injection capability. This leads to a more expensive DVR system. Economic feasibility of such a DVR system depends on the importance of the sensitive load protected by the DVR and the cost of the DVR itself.

The performance of the proposed control scheme is evaluated through various simulation studies in the PSCAD/EMTDC platform. The study results indicate that the proposed control strategy:1)limits the fault current to less than the nominal load current and restores the PCC voltage within less than10ms,and interrupts the fault current within two cycles; 2) it can be used in four- and three-wired distribution systems, and single-phase configurations;3)doesnotrequirephase-lockedloops;4)Is not sensitive to noise, harmonics, and disturbances and provides effective fault current interruption even under arcing fault conditions; and 5) can interrupt the downstream fault current under low dc-link voltage conditions.

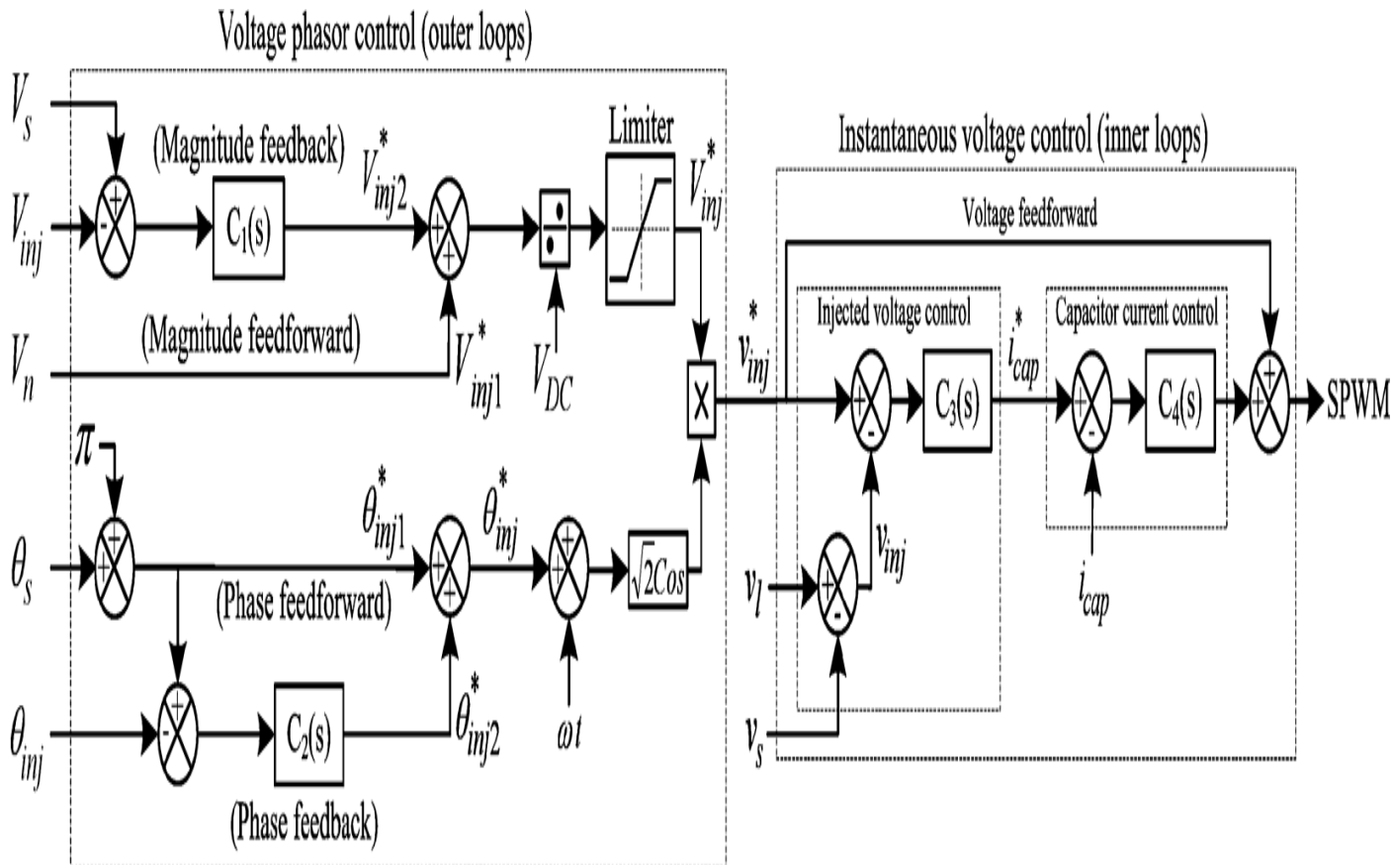

Fig. 2. Per-phase block diagram of the DVR control system in FCI mode.

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II. PROPOSED FCI CONTROLSTRATEGY

The adopted DVR converter is comprised of three independent H-bridge VSCs that are connected to a common dc-link capacitor. These VSCs are series connected to the supply grid, each through a single-phase transformer. The proposed FCI control system consists of three independent and identical controllers one for each single-phase VSC of the DVR.

Assume the fundamental frequency component sof the supply voltage , load voltage , and the injected voltage , Fig. 1 are

$$v_s = V_s \times \cos(\omega t + \theta_s). \quad (1)$$
$$v_l = V_l \times \cos(\omega t + \theta_l). \quad (2)$$
$$v_{\text{inj}} = v_l - v_s = V_{\text{inj}} \times \cos(\omega t + \theta_{\text{inj}}). \quad (3)$$

Two identical least error squares (LES) filters [14] are used to estimate the magnitudes and phase angles of the phasors corresponding to $v_s$and v_{inj} (i.e., $= V_s\angle\theta_s$and $\overrightarrow{V_{inj}} = V_{inj}\angle\theta_{inj}$, respectively in 5 ms[13]).

The FCI function requires a phasor parameter estimator (digital filter) which attenuates the harmonic contents of the measured signal. To attenuate all harmonics, the filter must have a full-cycle data window length which lead stone cycle delay in the DVR response.Thus, acompromise between the voltage injection speed and disturbance attenuation is made. The designed LES filters utilize a data window length of 50 samples at the sampling grate of 10kHzand,hence, estimate the voltage phasor parameter sin5ms.Fig.3depicts the frequency response of the LES filters and indicates significant attenuation of voltage noise, harmonics, and distortions at frequencies higher than 200 Hz and lower than 50 Hz. Reference [13] demonstrates the effectiveness of this filter in attenuating the noise, harmonics, and distortions for thesag compensation mode of operation as well. The next section shows that this filter also performs satisfactorily in the FCI operation mode, even under arcing fault conditions where them easured voltage and current signals are highly distorted.

Fig.2showsaper-phaseblockdiagramoftheproposedDVR control system corresponding to the FCI operation mode, where$V_n$is the nominal rms phase voltage. The control system of

Fig. 2 utilizes , , the dc-link voltage V_{DC}, and the harmonic filter capacitor current i_{cap}as the input signals. The reported studies in this paper are based on the over current fault detection method of[7] and [12]. The fault detection mechanism for each phase is activated when the absolute value of the instantaneous current exceeds twice the rated load current.

The proposed multiloop control system[3],[8],[9],[15]–[20] includes an outer control loop (voltage phasor control) and an inner control loop (instantaneous voltage control). The inner loop provides damping for the transients caused by the DVR harmonic filter [18] and [21], and improves the dynamic Response and st ability of the DVR. The inner loop is shared by the sag compensation and the FCI functions. When a downstream fault is detected, the outer loop controls the injected voltage magnitude and phase angle of the faulty phase(s) and reduces the load-side voltage to zero, to interrupt the fault current and restore the PCC voltage. The DVR" outer" voltage phasorcon troll and inner "instantaneous voltage control, corresponding to each phase, are described in the following two subsections.

A. Voltage Phasor Control System

In the FCI operation mode, the required injected voltage phasor is equal to the source voltage phasor, but in phase opposition [i.e., the injected phasor$\overrightarrow{V_{\text{inj}}} = V_{\text{inj}}\angle\theta_{\text{inj}}$is controlled to be $V_s\angle(\theta_s + \pi)$]. Performance of the voltage phasor control, in terms of transient response, speed, and steady-state error, is enhanced by independent control of voltage magnitude and phase, and incorporating feed forward signals to the feedback control system [17], [18], [21]–[27]. Fig. 2 shows two propor tional-integral (PI) controllers ($C_1$and C_2) that are used to eliminate the steady-state errors of the magnitude and phase of the injected voltage, respectively. Parameters of each controller

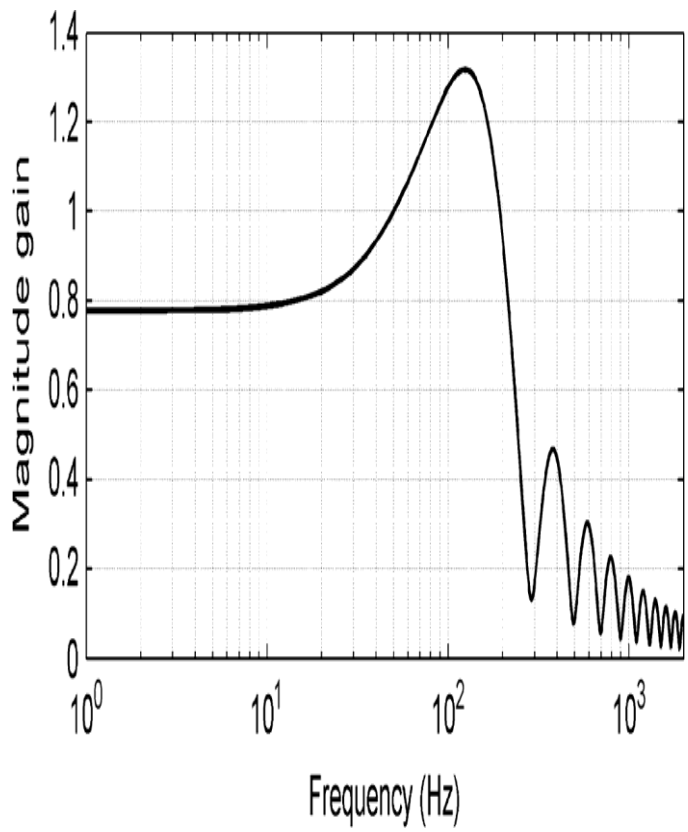

Fig. 3. Magnitude of the LES filters frequency response.

Are determined to achieve a fast response with zero steady-state error.

The output of the phas or control system is ference phas or denoted by $\overrightarrow{V_{inj}^*} = V_{inj}^* \angle \theta_{inj}^*$. To eliminate the effects of the dc-link voltage variations on the injected voltages, V_{inj}^* is normalized by V_{DC}. The magnitude and the phase angle of $\overrightarrow{V_{inj}^*}$ are independently calculated and the magnitude is passed througha limiter(Fig.2).There sulting phasor magnitude and phase angle are converted to the sinusoidalsignal v_{inj}^*, which is the reference signal for the instantaneous voltage control.

B. Instantaneous Voltage-Control System

Underidealconditions,avoltagesagcanbeeffectivelycompensated if the output of the phasor-based controller v_{inj}^* is directly fed to the sinusoidal pulse-width modulation (SPWM) unit.However,resonancesoftheharmonicfiltercannotbeeliminatedundersuchconditions.Therefore,toimprovethestability and dynamic response of the DVR, an instantaneous injected voltage controller and a harmonic filter capacitor current controller are used to attenuateresonances.

The generated reference signal for theinjectedvoltage v_{inj}^* is compared with the measured injected voltage v_{inj}, and the error is fed to the voltage controller. As shown in Fig. 2, the output of the voltage controller i_{cap}^* is the reference signal for thefiltercapacitorcurrentcontrolloop.Itiscomparedwiththe measured capacitor current i_{cap}, and the error is fed to the currentcontroller.

Thesteady-stateerroroftheproposedcontrolsystemisfully eliminatedbythePIcontrollersintheoutercontrolloop(i.e.,$C_1$and C_2), which track dc signals (magnitude and phase angle). Therefore, there is no need for higher order controllers in the inner control loop which are designed based on sinusoidal references. Thus, in Fig. 2, $C_3$and $C_4$are pure gains $k_i$and k_c, respectively.

A large $k_i$results in amplification of the DVR filter reso nance and can adversely impact the systems t ability[18].Thus, the transient response of the DVR is enhanced by a feed forward loop, and a smallproportionalgainisutilizedas the voltage con- troller. A largek$_c$damps the harmonic filter resonance more effectively, but it is limited by practical considerations (e.g., amplification of capacitor current noise, measurement noise, and dc offset [18]). Therefore, the lowest value of the propor- tional gain which can effectively damp the resonances is uti- lized. The output of the current controller is added to the feed- forward voltage to derive the signal for the PWMgenerator.

III. STUDYRESULTS

Fig. 4 depicts a single-line diagram of a power system which is used to evaluate the performance of the proposed DVR control system under different fault scenarios, in the PSCAD/EMTDC software environment. A 525-kVA DVR system is installed on the 0.4-kV feeder, to protect a500-kVA, 0.90 lagging power factor load against voltage sags. Parameters of the simulated power system and the DVR are given in Appendix A. In the reported studies, the base voltage for per-unitvaluesisthenominalphasevoltage.Besides,voltage

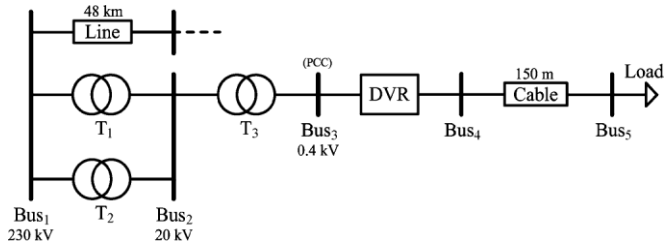

Fig. 4.Single-line diagram of the system used for simulation studies.

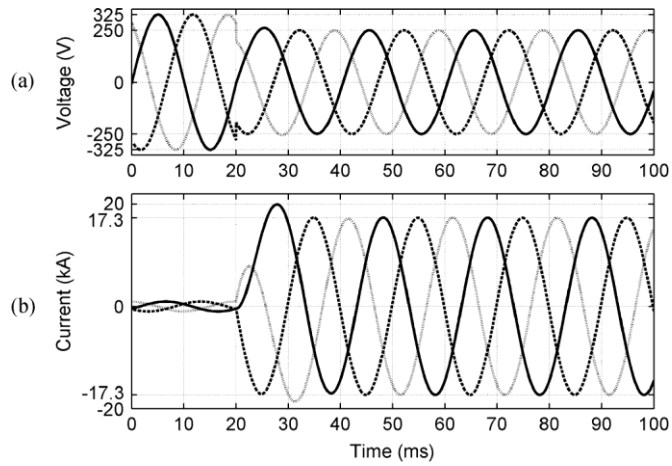

Fig.5.(a)VoltagesatBus_3.(b)Faultcurrents,duringdownstreamthree-phase fault when the DVR is inactive(bypassed).

and current waveforms of phases A, B, and C are plotted by solid, dashes, and dotted lines, respectively.

A. Three-Phase DownstreamFault

The system is subjected to a three-phase short circuit with a negligible fault resistance at $t = 20$ ms at Bus_5. Prior to the faultinception,theDVRisinactive(instandbymode)(i.e.,the primary windings of the series transformers are shorted by the DVR). During the fault if the DVR is bypassed, the voltage at Bus3 drops to 0.77 p.u. and the fault current increases to about17timestheratedloadcurrent(Fig.5).Fig.6showsFCI performance of the proposed DVR control system during the fault.Fig.6(a)–(c),respectively,showsthethree-phaseinjected voltages,therestoredthree-phasesupply-sidevoltages,andthe three-phase load-side voltages which are reduced to zero to interrupt the fault currents. The slightly injected voltage by the DVR before the fault initiation [Fig. 6(a)] is the voltage drop acrosstheseriesimpedanceoftheDVRseriestransformersecondarywinding.

Fig. 6(d) shows the line currents (i.e., the currents passing through the DVR). Fig. 6(d) illustrates that the proposed FCI methodlimitsthemaximumfaultcurrenttoabout2.5timesthe nominal value of the load current and interrupts the fault currents in less than 2 cycles. Fig. 6(e) depicts variations of the dc-link voltage during the FCI operation, and indicates that the dc-link voltage rise under the worst case (i.e., a severe three-phase fault) is about 15% and occurs during the first 5 ms after faultinception.

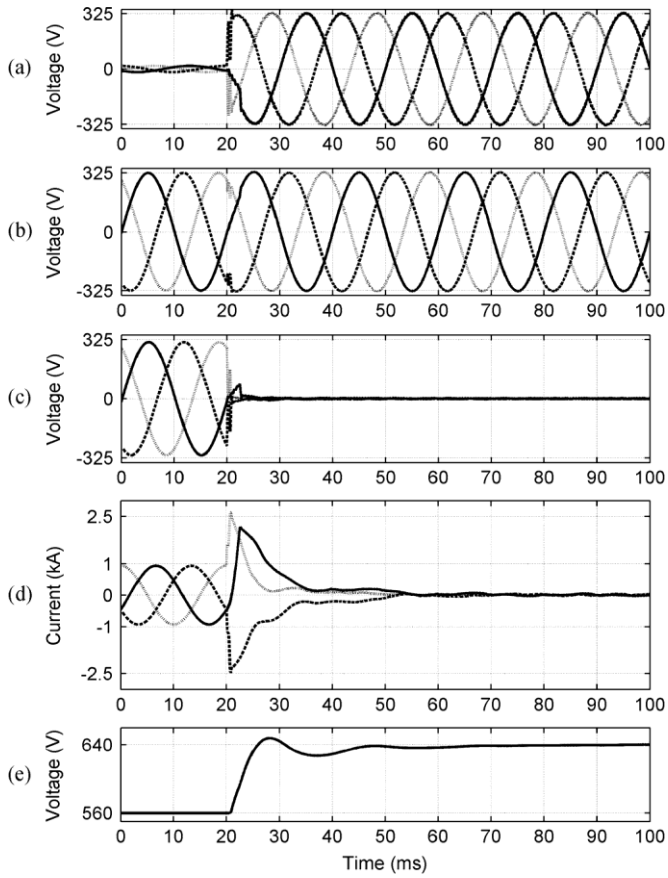

Fig. 6. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the three-phase downstream fault.

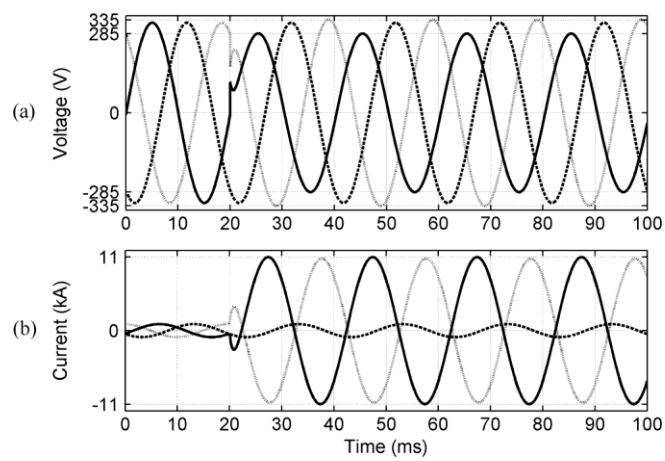

Fig. 7. (a) Voltages at Bus_3, (b) Fault currents, during downstream phase-to-phase fault when the DVR is inactive(bypassed).

B. *Phase-to-Phase DownstreamFaults*

The system of Fig. 4 is subjected to a phase-A to phase-C fault with the resistance of 0.05 Ω at 10% of the cable length connecting Bus_4 to Bus_5, at 20 ms. When the DVR is inactive (bypassed) during the fault (Fig. 7), the PCC voltage drops to 0.88 p.u., and the fault current increases to about 11 times the rated loadcurrent.

Fig. 8 illustrates that when the DVR is in service, the proposed FCI control successfully interrupts the fault current and

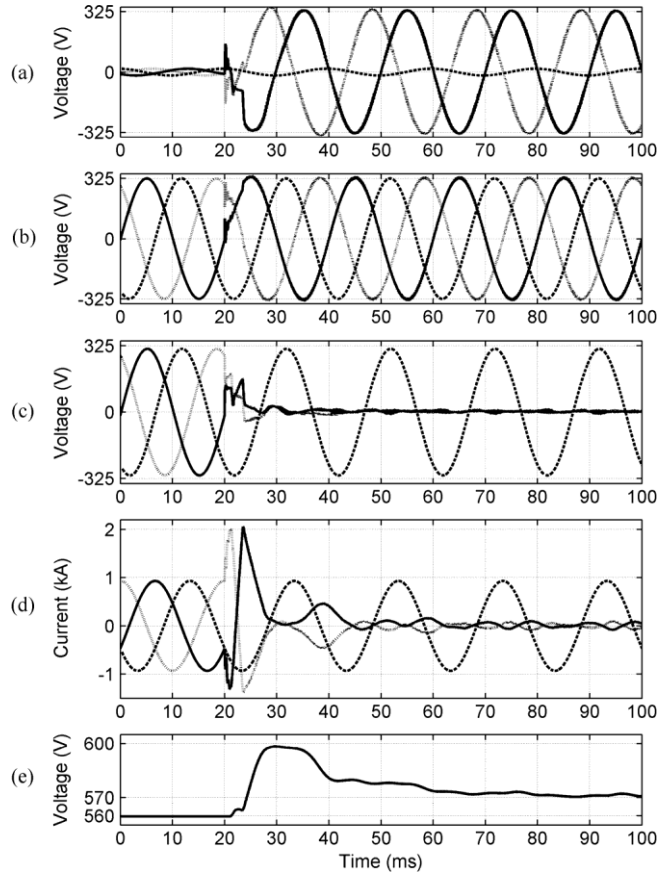

Fig. 8. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the phase-to-phase downstream fault.

restoresthePCCvoltageofthefaultyphaseswithintwocycles. Fig. 8(e) shows that the dc-link voltage rise is less than 7%. Fig. 8 also shows that only the two faulty phases of the DVR react, and the healthy phase is notinterrupted.

C. *Single-Phase-to-Ground DownstreamFault*

Phase-A of the system of Fig. 4 is subjected to a fault with theresistanceof0.2 Ωat10%lengthofthecableconnecting$Bus_4$to Bus_5, at 20 ms. If the DVR is inactive (Fig. 9), the PCCvoltagedoesnotconsiderablydropandthefaultcurrentis about 2.5 p.u. It must be noted that although the PCC voltage drop is not considerable, the fault current must be interrupted bytheDVRtopreventpossibledamagestotheVSCbeforethe faultisinterruptedbytherelays.Thereasonisthattheoperation timeoftheovercurrentrelaysisconsiderableforafaultcurrent of about 2.5p.u.

Fig. 10 illustrates that the proposed DVR control strategy successfully interrupts the fault current in the faulty phase in abouttwocycles.Fig.10(e)showsthatthedc-linkvoltagerises less than 1.8%. Fig. 10 also shows that only the faulty phase of the DVR reacts to fault current, and the healthy phases are not interrupted.

Simulation studies conclude that the dc-link voltage rise caused by the proposed FCI mode of operation is proportional tothefaultcurrent,anddependsonthetypeoffault.Theresults also indicate that the maximum dc-link voltage riseoccurs

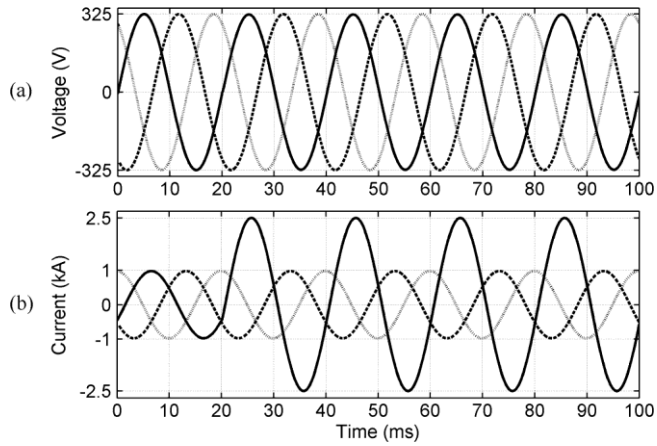

Fig. 9. (a) Voltages at Bus_3. (b) Fault currents, during the downstream single-phase-to-ground fault when the DVR is inactive(bypassed).

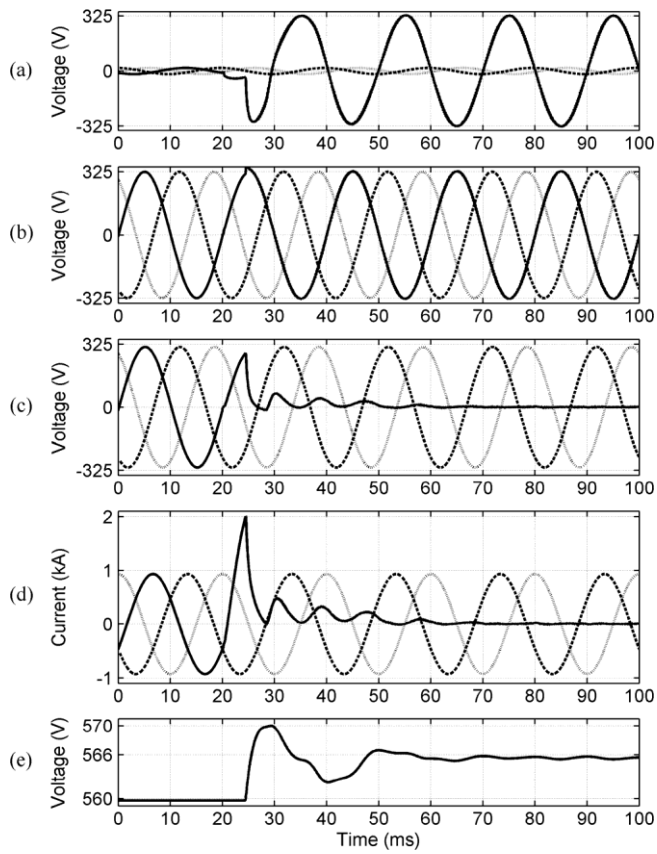

Fig. 10. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the single-phase-to-ground downstream fault.

under the most severe three-phase fault which is about 15%, and can be tolerated based on DVR appropriate design.

It must be noted that to prevent operation of three-phase induction motors under unbalanced voltage conditions, they must be equipped with protective devices which detect such conditions and disconnect the load when any of the phases is de-energized by the single-phase operation of the FCI function. Furthermore, disabling the single-phase fault current interruption capability can be provided as an operational option and the operator can decide either to use or disable this function depending on the type of load.

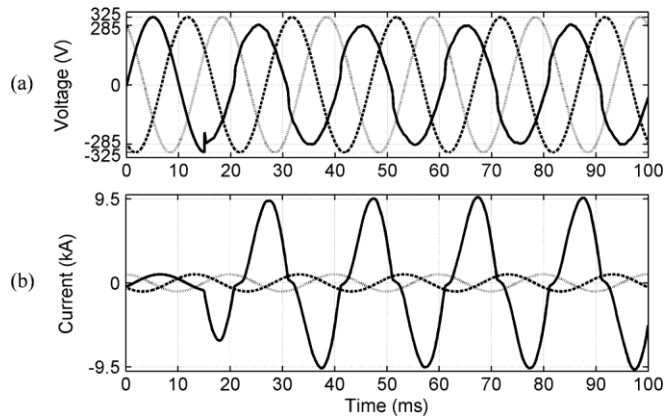

Fig.11.(a) Voltages at Bus_3.(b)Fault currents, during the downstream single- phase-to-ground arcing fault when the DVR is inactive(bypassed).

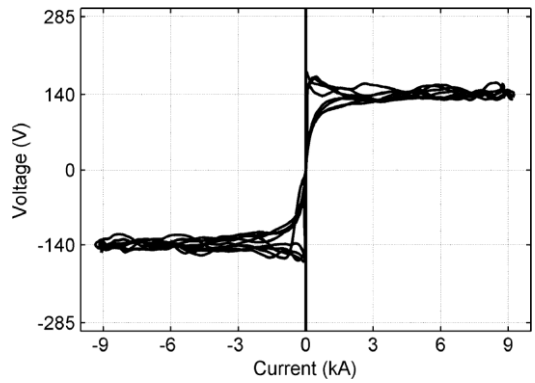

Fig. 12.Nonlinear - characteristic of the arc.

D. *Effect of the Fault v-iCharacteristic*

Due to the nonlinear v-i characteristic of a free-burning arc, the voltage and current waveforms are highly distorted during an arcing fault. To investigate the effects of such distortions on the performance of the proposed FCI control scheme, a single-phase-to-ground downstream arcing fault at Bus_5 is considered. The arc is modeled based on the modified Cassie–Mayre equations [28]. The effect of variation of the arc length on the arc voltage [29] is also taken into account.

The fault is initiated at t = 15 ms on phase A. When the DVR is inactive (bypassed), Fig. 11, the PCC voltage drops to 0.87 p.u., and the fault current rises to about 9.5 p.u. Fig. 12 shows the time-varying nonlinear v-i characteristic of the arc during this fault. Fig. 11 shows the PCC voltage, and the fault current waveforms are highly distorted as a result of the fault v-i characteristic. This is confirmed by the frequency spectrum of the voltage waveform as depicted in Fig. 13.

The performance of the proposed FCI control scheme during the arcing fault is illustrated in Fig. 14. Fig. 14 shows that the proposed control strategy successfully interrupts the arcing fault current in the faulty phase in half a cycle (i.e., even faster than that of the bolted fault conditions). The reason is that the resistance of the arcing fault provides higher damping for the decaying dc component of the fault current.

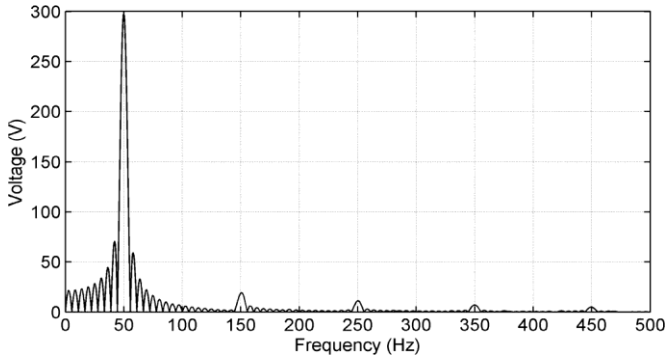

Fig. 13.Harmonic content of voltage at Bus_3during the arcingfault.

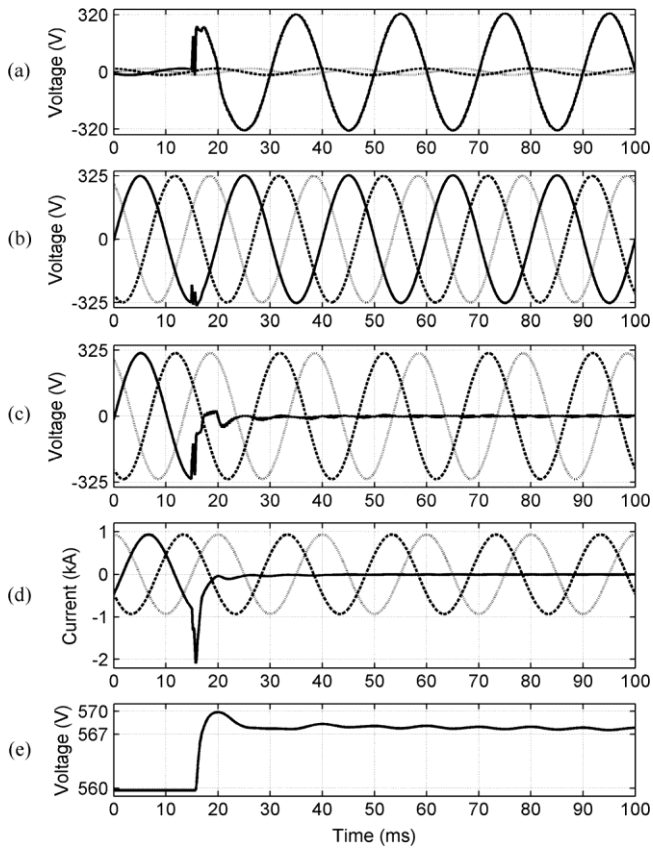

Fig. 14. (a) Injected voltages. (b) Source voltages. (c) Load voltages. (d) Line currents. (e) DC-link voltage, during the single-phase-to-ground downstream arcing fault.

E. Simultaneous FCI Operation and Sag Compensation

The proposed DVR control system performs two different functions (i.e., sag compensation and FCI). Thus, the mutual effects of these modes on each other must be evaluated. At $t = 15$ms,thesystemofFig.4issubjectedtoaphase-Atophase-B faultwiththeresistanceof1 Ωat90%ofthelinelengthfromBus_1 .Thefaultcauses87%voltagesagatthePCC.At $t = 55$ ms, another fault with the resistance of 0.2Ωon phase-A at 10% length of the cable connecting Bus_4 to Bus_5occurs. The upstream fault is cleared by relays at 93ms.

Fig.15showstheperformanceoftheproposedDVRcontrol system under the a fore mentioned conditions(i.e., simultaneous FCI operation and sag compensation).Fig.15showsthatwhen

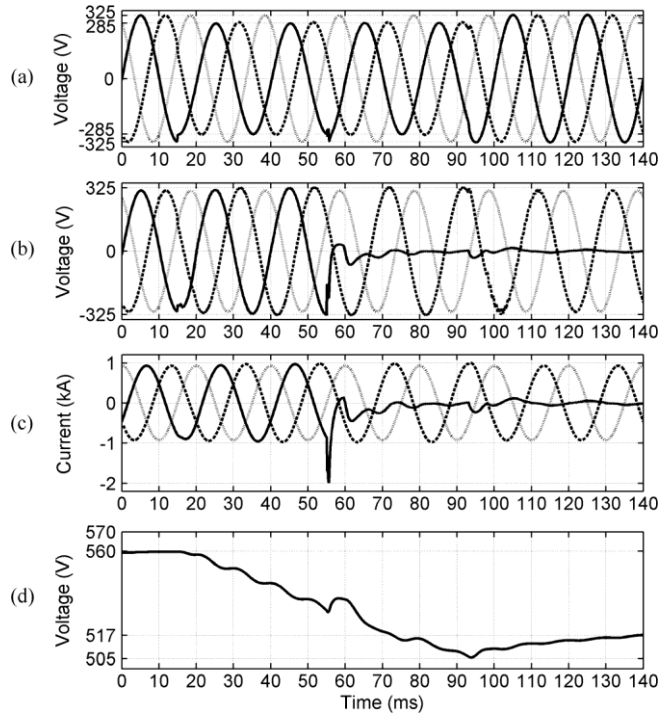

Fig. 15. (a) Source voltages. (b) Load voltages. (c) Line currents. (d) DC-link voltage, during phase-A to ground downstream fault which takes place during sag compensation in phases A and B.

the downstream fault occurs in phase-A, the operation mode of theDVRinphase-A changes from sagcompensationto FCI operation. However, the DVR continues to compensate the sag in phase-B to restore the load voltage in th is phase. Consequently, phase-A and phase-B of the DVR operate in sag compensation modeduring$15 < t < 55$ ms.During$55 < t < 93$ ms, phase-A is in FCI operation mode, and phase-B continues to compensate the sag. During93 ms, phase-B is in standby mode since the upstream fault is cleared and phase-A continues to interrupt the downstream fault current. During the entire process,phase-Cis in standbymode.

Fig. 15(d) depicts variations of the dc-link voltage and indicates that the dc-link voltage drops during sag compensation, but the FCI operation maintains the dc-link voltage when it is lower than a certain value(thedc-link voltage, which is needed to reduce the load voltage to zero). This continues until the capacitor voltage approaches the aforementioned threshold. The reason is th at when the capacitor voltage is lower than a certain value,themagnitude of thevoltageinjectedbytheDVR, which must be 180° out of phase with respect to the source voltage, is less than the source voltage magnitude. Thus, small current flowst hrough the DVR until the capacitor is charged. This cur rent results in active power absorption by theDVR.

Fig. 16 shows the effect of lower initial dc-link voltage on the FCI operation during a phase-A to ground fault with the resistance of 0.05Ωat 10% length of the cable connecting$\mathrm{Bus}_4$to Bus_5, at 15 ms. If the DVR is inactive (bypassed) during the fault, the fault current increases to about 7 times the rated loadcurrent.Fig.16(a)shows that even under very low dc-link voltage conditions, the FCI control limits the fault current to lessthanthenominalloadcurrentinaboutonecycle.Fig.16(b)

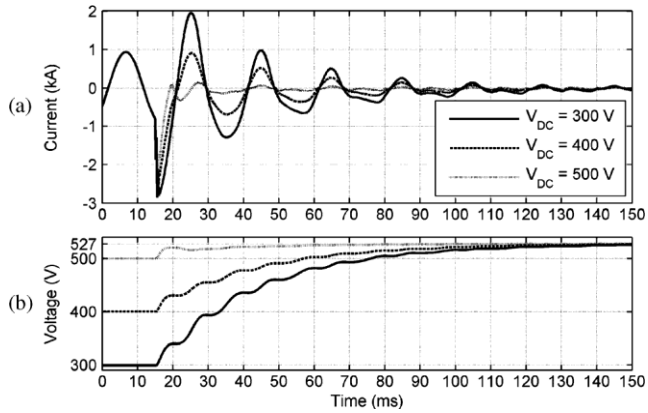

Fig.16.(a)Linecurrentofphase-Aand(b)dc-linkvoltage,fordifferentinitial values of the dc-link voltage, during downstream phase-A-to-ground fault.

shows that regardless of the initial dc-link voltage, the dc-link capacitor is charge dup to a voltage which is adequate to inject a voltage equal to the supply voltage and fully interrupt the fault current.

IV. Conclusion

This paper introduces an auxiliary control mechanism to enable the DVR to interrupt downstream fault currents in a radial distribution feeder. This control function is an addition to the voltage-sag compensation control of the DVR. The performance of the proposed controller, under different fault sce- narios, including arcing fault conditions, is investigated based on time-domain simulation studies in the PSCAD/EMTDC environment. The study results conclude that:

- The proposed multiloop control system provides a desirable transient response and steady-state performance and effectively damps the potential resonant oscillations caused by the DVR LC harmonic filter;
- the proposed control system detects and effectively interrupts the various downs tream fault currents with intwocy cles (of 50Hz);
- the proposed fault current interruption strategy limits the DVR dc-link voltage rise, caused by active power absorption, to less than 15% and enables the DVR to restore the PCC voltage without interruption; in addition, it interrupts the down stream fault currents even under low dc-link voltage conditions.
- the proposed control system also performs satisfactorily under downstream arcing fault conditions.

Appendix A
DVR Model Parameters

Parameters of the studied power system and the DVR are as follows.

short-circuitcurrentatBus_1:31.5kA,X/RatBus_1 ; 5.67
$\omega = 2\pi \times 50\,\mathrm{rad/s}$;
transmission line (48 km):

$$R_{\mathrm{Line}} = 1.876\,\Omega,\ L_{\mathrm{Line}} = 0.0774\ \mathrm{H};$$

TABLE I
Transformer Parameters

Transformer	T_1, T_2	T_3	T_s
Rated Power (MVA)	90	2	0.175
No load losses (p.u.)	0.001	0.00205	0.003
Copper losses (p.u.)	0.0048	0.0097	0.02
Leakage reactance (p.u.)	0.237	0.06	0.05
Primary voltage rating (kV)	230	20	0.4
Secondary voltage rating (kV)	20	0.4	0.245
Winding connection type	YnD	DYn	---

TABLE II
VSC Parameters

Parameter	Value
Switching frequency (unipolar SPWM)	3 kHz
DC-link rated voltage	560 V
DC-link capacitor	100 mF
Harmonic filter capacitor C_f	300 μF
Harmonic filter inductor L_f (leakage inductance of T_s)	56.82 μH

cable (150 m):

$$R_{\mathrm{cable}} = 9.6\ \mathrm{m}\Omega,\ L_{\mathrm{cable}} = 340\ \mathrm{mH}.$$

Parameters of the step-down transformers T_1, T_2, and T_3, and the DVR series transformers $T_s$are given in Table I. Parameters of the VSC are given in TableII.

In FCI operation mode, each single-phase series transformer should be able to inject 1-p.u. line-to-neutral voltage (231 V). Taking into account the voltage drop across its series branch impedance under the nominal load current of 721 A and the safety margin needed to prevent over modulation during transients, the secondary voltage rating of the series transformer is chosen to be 245 V. Therefore, the power rating of$T_s$is $245\ \mathrm{V} \times 721\ \mathrm{A} \approx 175$ kVA, and the rating of the DVR is $3 \times 175 = 525$ kVA.

The controller transfer functions are as follows:

$$C_1(s) = k_{p1} + \frac{k_{I1}}{s}, \quad k_{p1} = 0.2k_{I1}100 =$$
$$C_2(s) = k_{p2} + \frac{k_{I2}}{s}, \quad k_{p2} = 0.1k_{I2} = 500$$
$$C_3(s) = k_c = 0.1$$
$$C_4(s) = k_c = 0.7$$

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