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DESIGN AND IMPLEMENTATION OF 64 BIT HIGH SPEED VEDIC MULTIPLIER

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Abstract:- Multiplier is one of the key hardware blocks in most digital signal processing (DSP) systems. Typical DSP applications where a multiplier plays an important role include digital filtering, digital communications and spectral analysis. Many current DSP applications are targeted at portable, battery-operated systems, so that power dissipation becomes one of the primary design constraints. Since multipliers are rather complex circuits and must typically operate at a high system clock rate, reducing the delay of a multiplier is an essential part of satisfying the overall design.. This paper puts forward a high speed multiplier ,which is efficient in terms of speed, making use of UrdhvaTiryagbhyam[1], a sutra from Vedic Maths for multiplication and half adder for addition of partial products. The code is written in VHDL and results shows that multiplier implemented using Vedic multiplication is efficient in terms of area and speed compared to its implementation using Array and Booth multiplier architectures.

Keywords: *Half adder, Array multiplier, Booth's Multiplier, Vedic Multiplier, Vedic Mathematics.*

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I INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used computation Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit. Multiplication can be implemented using several algorithms such as: array, Booth, modified Booth algorithms. Array multiplier is well known due to its regular structure. Multiplier circuit is based on add and shift algorithm. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. The partial product are shifted according to their bit orders and then added. Booth Multipliers is a powerful algorithm for signed-number multiplication, which treats both positive and negative numbers uniformly. This method that will reduce the number of multiplicand multiples. For a given range of numbers to be represented, a higher representation radix leads to fewer digits. The partial-sum adders can also be rearranged in a tree like fashion, reducing both the critical path and the number of adder cells needed. The presented structure is called the Wallace tree multiplier The tree multiplier realizes substantial hardware savings for larger multipliers. The propagation delay is reduced as well. In fact, it can be shown that the propagation delay through the tree is equal to O (log3/2 (N)). While substantially faster than the carry-save structure for large multiplier word lengths, the Wallace multiplier has the disadvantage of being vary irregular, which complicates the task of an efficient layout design.

II LITERATURE SURVEY

Rapidly growing technology has raised demands for fast and efficient real time digital signal processing applications. Multiplication is one of the primary arithmetic operations every application demands. A large number of multiplier designs have been developed to enhance their speed. Active

research over decades has lead to the emergence of Vedic Multipliers as one of the fastest and low power multiplier over traditional array and booth multipliers. Honey Durga Tiwari.et.al talked about designing a multiplier and square architecture is based on algorithm of ancient Indian Vedic Mathematics, for low power and high speed applications. They explained Urdhvatiryakbhyam and Nikhilam algorithm and found that Urdhvatiryakbhyam, is applicable to all cases of multiplication but due to its structure, it suffers from a high carry propagation delay in case of multiplication of large numbers. This problem has been solved by introducing Nikhilam Sutra which reduces the multiplication of two large numbers to the multiplication of two small numbers. Prof J M Rudagil.et.alldesigned a multiplier using vedic mathematics. They explained Urdhvatiryakbhyam and found that it is efficient Vedic multiplier with high speed, low power and consuming little bit wide area was designed. It was also found that the multiplier based on vedic sutras had execution delay of almost half of that of binary multiplier. Sree NivasA .et.all presented a technique that modifies the architecture of the Vedic multiplier by using some existing methods in order to reduce power. They explained Nikhilam sutra and double base number system. Nikhilam sutra method is not valid for negative numbers. They found that Vedic Multiplier without any Modification has high power consumption. Vedic Multiplier with modified Two's complement block has less power consumption with cost of delay and area. Full adders are designed for a 16-bit vedic multiplier to decrease number of slices and delay. The results obtained are compared and it is found that the reformed full adders have less delay. The design is implemented using four adders of different techniques such as full adder using two half adders and an OR gate. Second modified full adder is designed by using XOR gate and 2:1 multiplexer, third modified full adder by using two 4:1 multiplexer and fourth modified full adder using a combination of XOR gate, XNOR gate and a 2:1 multiplexer. After comparing the results, they concluded that the third modified full adder has better performance [3]. Gate diffusion input (GDI) is a method used for describing the structure of low-power digital combinatorial circuit. Consumption of power, delay that is produced and complexity of the circuit are reduced using this technique; thereby it maintains less complexity in logical layout. The GDI technique is implemented using two transistors for a deep range of complex logic design [4]. A high speed 32-bit vedic multiplier is designed. For addition of partial products in a 32-bit vedic multiplier Kogge stone adder and a ripple carry adder is used. Two multipliers are implemented using these two methods and results are compared with these two multipliers [5]. In 8-bit multiplier which is implemented using Urdhva Tiryagbhyam sutra, the partial product addition is realized using carry skip technique. A digital processor requires a multiplier as it is a basic block in the processor [6]. A 32-bit vedic multiplier is proposed using one carry save adder. The input of multiplier is arranged in two 16-bit numbers to apply it stepwise using Urdhva Tiryagbhyam sutra and the partial product is added using one carry save adder thus reducing the hardware blocks in the circuit [7]. The processors are integrated into one chip as demand of complex processors is increased. But the load on the processor is not reduced. To reduce this load, the main processor is equipped with co-processors [8]. Design of a hybrid FIR filters using vedic multipliers and fast adders is todays need in many DSP processors. FIR filters play a significant role in the field of digital signal processors to eliminate noise suppression in electro cardio graph, imaging devices and the signal stored in analog media. So filter evaluation is accomplished to reduce the noise level. Multipliers and adders play a vital role in determining the performance of FIR filter. They have proposed modified Annuprya vedic multiplier methods with Kogge Stone fast adder for implementation in the direct form FIR filter [9]. Multipliers play a major role in today's digital signal processing and various other applications. Both signed and unsigned multiplications are required in many computing applications.

III PROPOSED SYSTEM

Vedic mathematics - a gift given to this world by the ancient sages of India. A system which is far simpler and more enjoyable than modern mathematics. The word "Vedic" is derived from the word "Veda" which means the store-house of all knowledge[1].Vedic math was rediscovered from the ancient Indian scriptures between 1911 and 1918 by Sri Bharati Krishna Tirthaji (1884-1960), a scholar of sanskrit, Mathematics, History and Philosophy.It is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upaveda (supplement) of AtharvaVeda[2]. Vedic mathematics is mainly based on 16 Sutras dealing with various branches of mathematics like arithmetic, algebra, geometry etc. These Sutras along with their brief meanings are enlisted below alphabetically[3].

I) (Anurupye) Shunyamanyat - If one is in ratio. The other is zero.

2) Chalana-Kalanabyham Differences and Similarities.

3) EkadhikinaPurvena - By one more than the previous one.

4) EkanyunenaPurvena - By one less than the previous one.

5) Gunakasamuchyah - The factors of the sum is equal to the sum of the factors.

6) Gunitasamuchyah - The product of the sum is equal to the sum of the product.

7) NikhilamNavatashcaramamDashatah - All from 9 and the last from 10.

8) ParaavartyaYojayet - Transpose and adjust.

9) Puranapuranabyham - By the completion or non completion.

10) Sankalana-vyavakalanabhyam - By addition and by subtraction.

11) ShesanyankenaCharamena - The remainders by the last digit.

12) ShunyamSaamyasamuccaye - When the sum is the same that sum is zero.

13) Sopaantyadvayamantyam - The ultimate and twice the penultimate.

14) Urdhva-tiryakbhyam - Vertically and crosswise.

15) Vyashtisamanstih - Part and Whole.

16) Yaavadunam - Whatever the extent of its deficiency

Proposed multiplier architecture of 64x64 bit vedic multiplier and major change adopted here is use of half adder for addition of partial products.

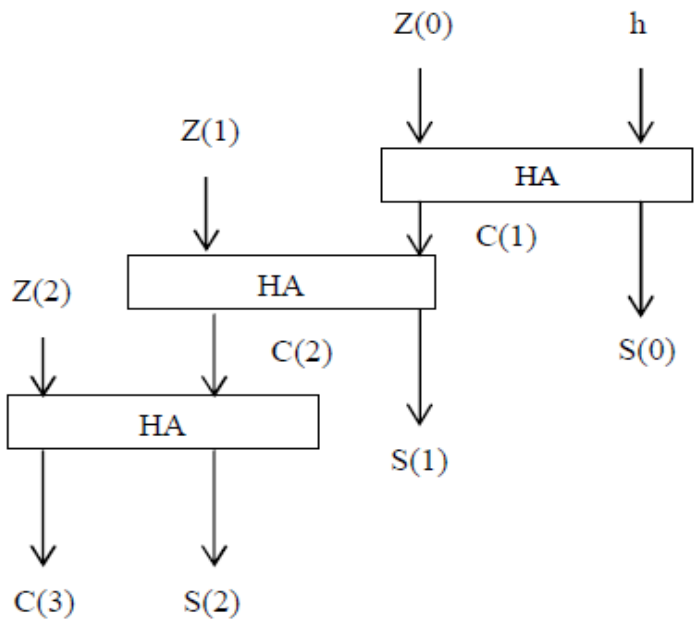

Figure 1: Addition of partial products with previous carry

The ancient vedic mathematics consists of a set of 16 sutras or main formulas and their 13 corollaries which can be efficiently used to solve mathematical calculations. One of the sutra is Urdhva Tiryagbhyam which means vertically and crosswise. This sutra can be used to perform a multiplication. The process of multiplication by using Urdhva Tiryagbhyam sutra is as follows, First step is to multiply the first digit that is left hand most digit of multiplicand with first digit of multiplier. The product is written as first digit in the answer. In second step multiply second digit of multiplicand with first digit of the multiplier and first digit of the multiplicand with second digit of multiplier, add the product. The result is written as second digit in the answer. Third step is to multiply second digit of multiplicand with second digit of multiplier, write the product as third digit in the answer.

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IV SIMULATION RESULTS AND DISCUSSION

Technology Schematic

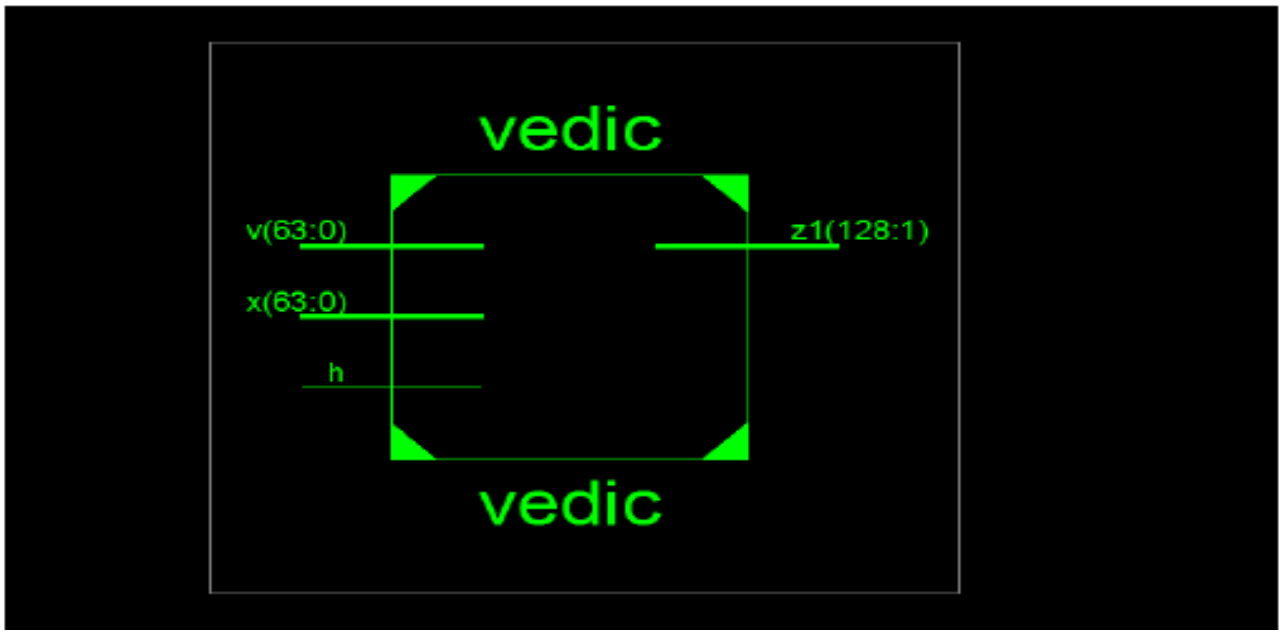

Figure 4. RTL schematic of 64 Bit VEDIC multiplier

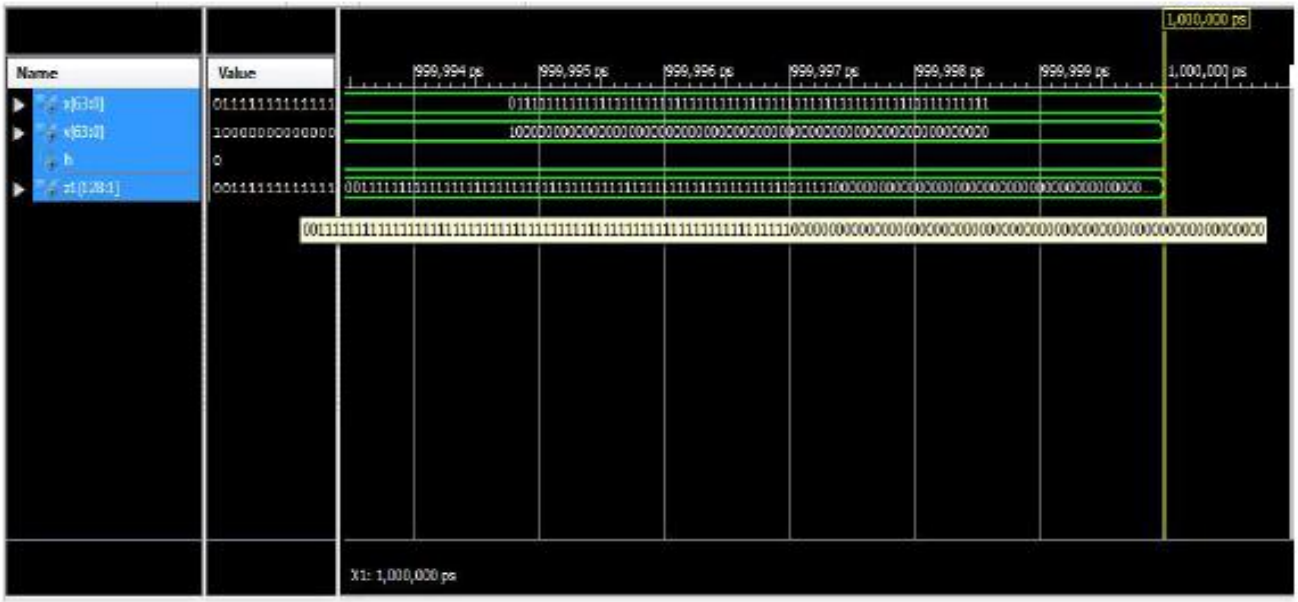

Figure 5. Simulation results 64 Bit VEDIC multiplier

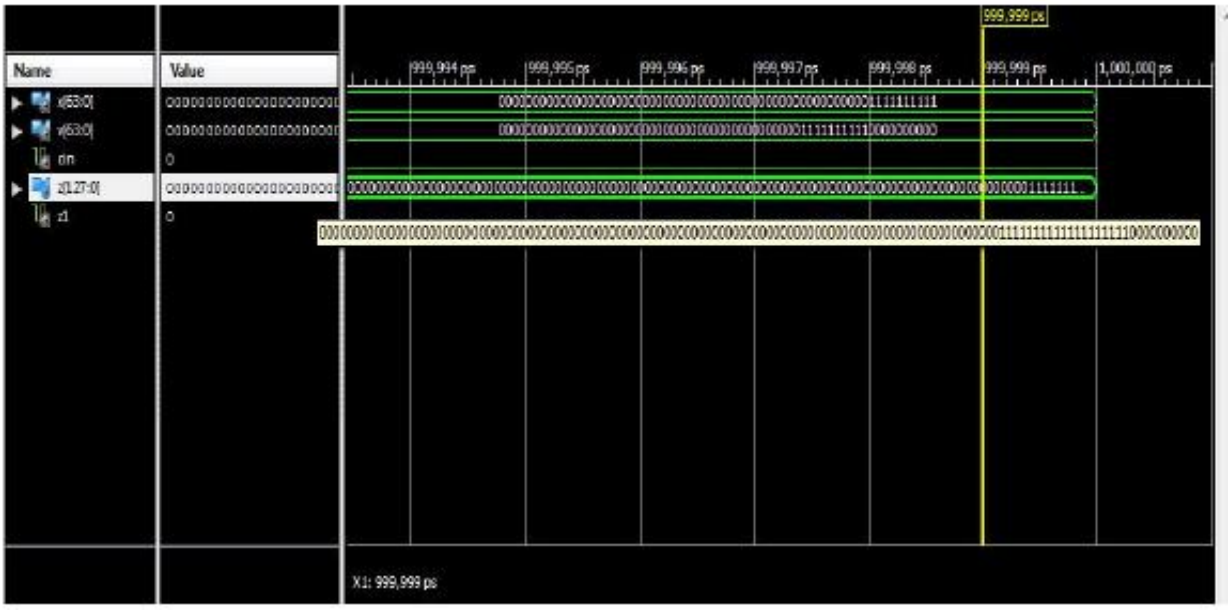

Figure.6. Simulation output of array multiplier

Timing Summery

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Timing Summary:
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Speed Grade: -12

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 29.967ns

Timing Detail:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 532354 / 128
-------------------------------------------------------------------------
Delay:               29.967ns (Levels of Logic = 47)
  Source:            x<4> (PAD)
  Destination:       z1<128> (PAD)

     ----------------------------------------
     Total                      29.967ns (10.624ns logic, 19.343ns route)
                                         (35.5% logic, 64.5% route)

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V CONCLUSION

A 64-bit vedic multiplier is designed by using Urdhva Tiryagbhyam Sutra of ancient vedic mathematics using VHDL and simulated on Xilinx ISE 14.7. The performance parameters like number of slice LUTs, number of bounded IOBs and combinational delay are analyzed and it is found that the number of slice LUTs used are 1758 out of 27288, number of bounded IOBs used are 128 and combinational delay is 54.037ns. The multiplier is designed using four 16-bit multiplier, one 32-bit full adder and two 48-bit full adders. The hardware requirement is large thus increasing the time delay. The basic building blocks should be reduced to achieve less time delay. The work can be extended to the adders used can be remodified using basic gates and multiplexer.

REFERENCES

[1] Vaijyanath Kunchigi, Linganagouda Kulkarni, Subhash Kulkarni, "High Speed and Area Efficient Vedic Multiplier", IEEE, Devices, Circuits and systems,Vol.4,pp.360-

364,15-16 March 2012.

[2] Ramachandran.S, Kirti.S.Pande , "Design, Implementation and Performance Analysis of an Integrated Vedic Multiplier Architecture", International Journal Of Computational Engineering Research,Vol. 2, Issue No.3, pp. 697-703, May-June 2012,.

[3] Prof J M Rudagil, Vishwanath Amble, VishwanathMunavalli, "Design and implementation of efficient multiplier using vedic mathematics", Proc. of1nt. Con/, on Advances in Recent Technologies in Communication and Computing, pp.162-166, Nov 2011.

[4] Premananda B.S., Samarth S. Pai, Shashank B., Shashank S. Bhat, "Design and Implementation of 8-Bit Vedic Multiplier", International Journal of Advanced Research in Electrical,Electronics and Instrumentation Engineering,Vol. 2, Issue 12, December 2013.

[5] Neeraj Kumar Mishra, SubodhWairya, "Low Power 32×32 bit Multiplier Architecture based on Vedic Mathematics Using Virtex 7 Low Power Device", IJRREST,Vol,-2, Issue-2, June-2013.

[6] Poornima M, Shivaraj Kumar Patil, "Implementation of Multiplier using Vedic Algorithm", IJITEE, Vol.-2, Issue-6, May 2013.

[7] Honey DurgaTiwari, Ganzorig Gankhuyag, "Multiplier design based on ancient Indian Vedic Mathematics", IEEE, International SoC Design Conference, Vol.-2,pp.II- 65-II-68,24-25 Nov 2008.

[8]Sudeep. M.C, Sharath Bimba.M, "Design and FPGA Implementation of High Speed Vedic Multiplier", International Journal of Computer Applications, Vol. 90, Issue 16, March 2014.