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IMPACT OF UNEQUAL DC-LINK CURRENTS ON THE PERFORMANCE OF 5-LEVEL CURRENT-FED INVERTERS CONTROLLED BY SVPWM

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Abstract – **The performance of multilevel CFIs is significantly challenge by unequal DC-link currents. Variations in DC-link current magnitudes can cause distorted output waveforms, increased harmonic content and reduced system efficiency. Traditional control strategies, which assume balanced DC-link currents, may no longer be effective under these conditions. This paper focuses on developing strategies for selecting switching state vectors for multilevel CFIs operating under unequal DC-link currents. The goal is to minimize the impact of current imbalance on the output waveform quality and overall system performance. The proposed strategies aim to ensure effective time sharing among switching states, optimize the distribution of current stress, and the goal is to minimize the of lower order-frequency harmonics in the output**

Keywords *– Current Fed, Multilevel Inverter, SVPWM, Switching State Vectors, Unbalanced*

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I INTRODUCTION

Multilevel Current-Fed Inverters (CFIs) are becoming increasingly popular in contemporary power electronics because they produce high-quality output waveforms, enhance efficiency, and minimize harmonic distortion [1-2] These advantages make them ideal for applications like RES [7], electric vehicles, and industrial drives. In a typical multilevel CFI, multiple DC sources [9] are employed to generate the desired output voltage levels. However, in practical implementations, these DC sources can experience imbalances, leading to unequal DC-link currents

1.1 Operation with Asymmetric DC-Link Currents

Differences in DC-link currents remove redundancy in switching state vectors, making all 49 vectors independent and changing the space vector diagram. This diagram can adopt two general shapes depending on the degree of current inequality. As a result, the output current (ia) becomes distorted, straying from the anticipated five-level waveform. Low-frequency components emerge in the harmonic spectrum, and their magnitude increases with greater current inequality. Careful selection and time-sharing of switching state vectors can help mitigate these low-frequency components. Two approaches are suggested for choosing suitable switching state vectors to address these issues: Method 1 involves selecting the nearest switching state vectors [8], while Method 2 focuses on choosing vectors that eliminate low frequency pulsations.

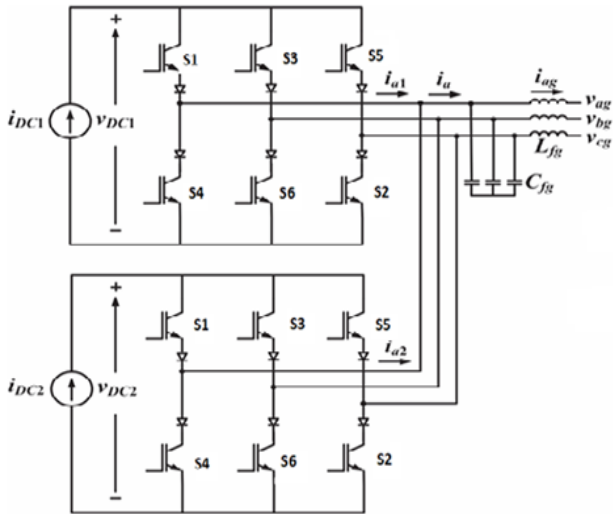

Figure 1: Fivel level Current Fed Inverter

The five-level space vector diagram can have two typical shapes based on the degree of inequality in DC-link currents of CFI units,[3-6] as illustrated in Figures 1 and 2.

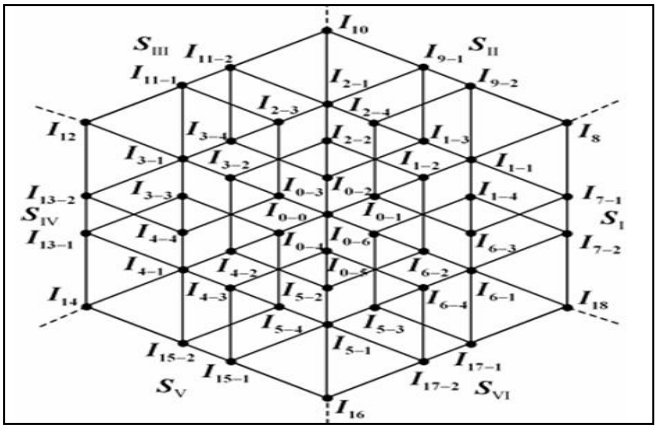

Figure 2: 0.5 < iDC1/ iDC2 < 2.

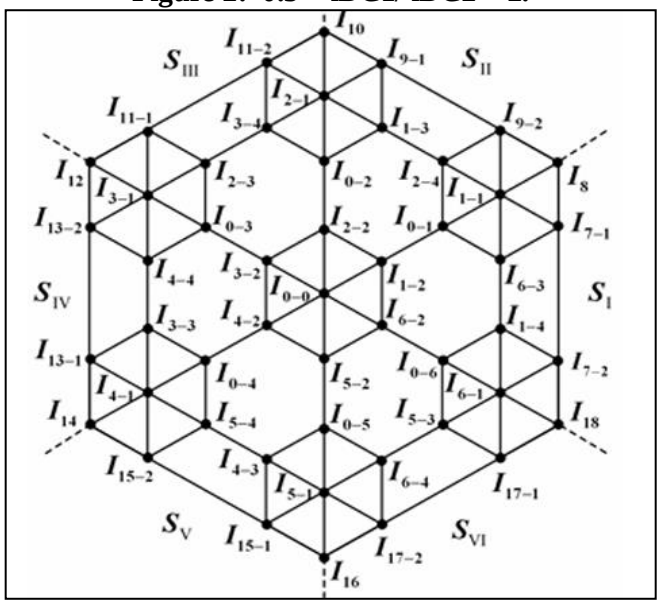

Figure 3: (iDC1/ iDC2 < 0.5) or (iDC1/ iDC2 > 2).

II METHOD 1: IDENTIFYING CLOSEST SWITCHING STATE VECTORS

The CFI unit carrying higher DC-link current is designated as CFI-1, while the other unit is designated as CFI-2. Each major sector (S_I–S_{VI}) contains 13 switching state vector positions and is further subdivided into 25 minor sectors.

.III METHOD 2: SELECTION OF SWITCHING STATE VECTORS TO ELIMINATE LOW-FREQUENCY PULSATION

The method eliminates low-frequency pulsations in vDC1 and vDC2 by avoiding specific switching state vectors in certain sectors. Despite this, the output current quality remains consistent, using 9 specific state vectors per major sector, unlike Method 1, and ensuring proper time-sharing between selected switching states.

Vectors I_{6-1}, I_{6-2}, I_{7-1}, I_{7-2}, I_8 ,$I_{18,}$ I_{0-0}, I_{1-1}, I_{1-2} are used in major sector S_I and active periods for thèse vectors are, T_{6-1}, T_{6-2}, T_{7-1}, T_{7-2}, T_8 , $T_{18,}$ T_{0-0}, T_{1-1}, T_{1-2} respectively. If $T_{6-1} = T_{6-2,}$ $T_{1-1}= T_{1-2}$, and $T_{7-1} = T_{7-2}$ The average DC-link voltage over each switching period can be calculated using the following formula,

$$v_{DC1} = v_{DC2} = 1.5m\, v_{ph} \cos\varphi$$

where, v_{ph} = phase voltage, m = modulation index &

cosφ = power factor.

The average DC-link voltage remains constant over each switching period, eliminating low frequency pulsations in v_{DC1} and v_{DC2}. A small L-C filter is used to eliminate the switching frequency component and achieve a ripple-free, constant voltage at the DC-DC converter output.

The reference space vector position is determined within minor sectors S1 to S4, bounded by fictitious state vector positions I1, I6, and I7 in major sector SI, as shown in Fig. 4

Table 1: Specific switching state vectors are selected for both major and minor sectors under Method 1

Major sector	Minor sector	Switching state vector			Switching states sequence									Number of switch transitions		
		x	y	z	$\frac{T_z}{4}$	-	T_x	-	$\frac{T_z}{2}$	-	T_y	-	$\frac{T_z}{4}$	CFI-1	CFI-2	Total
	S_1	I_{p-2}	I_{q-2}	I_{0-0}	(i_m, i_m)	-	(i_m, i_p)	-	(i_m, i_m)	-	(i_m, i_q)	-	(i_m, i_m)	0	8	8
	S_2	I_{p-2}	I_{q-2}	I_{0-p}	(i_p, i_w)	-	(i_m, i_p)	-	(i_p, i_w)	-	(i_m, i_q)	-	(i_p, i_w)	8	16	24
	S_3	I_{p-2}	I_{q-2}	I_{0-q}	(i_q, i_n)	-	(i_m, i_p)	-	(i_q, i_n)	-	(i_m, i_q)	-	(i_q, i_n)	8	16	24
	S_4	I_{p-2}	I_{q-2}	I_{0-p}	(i_p, i_w)	-	(i_m, i_p)	-	(i_p, i_w)	-	(i_m, i_q)	-	(i_p, i_w)	8	16	24
	S_5	I_{p-2}	I_{q-2}	I_{0-q}	(i_q, i_n)	-	(i_m, i_p)	-	(i_q, i_n)	-	(i_m, i_q)	-	(i_q, i_n)	8	16	24
	S_6	I_{0-p}	I_{0-q}	I_{p-2}	(i_m, i_p)	-	(i_p, i_w)	-	(i_m, i_p)	-	(i_q, i_n)	-	(i_m, i_p)	8	16	24
	S_7	I_{0-p}	I_{0-q}	I_{q-2}	(i_m, i_q)	-	(i_p, i_w)	-	(i_m, i_q)	-	(i_q, i_n)	-	(i_m, i_q)	8	16	24
	S_8	I_{0-p}	I_{0-q}	I_{q-4}	(i_p, i_v)	-	(i_p, i_w)	-	(i_p, i_v)	-	(i_q, i_n)	-	(i_p, i_v)	4	12	16
	S_9	I_{0-p}	I_{0-q}	I_{p-3}	(i_q, i_u)	-	(i_p, i_w)	-	(i_q, i_u)	-	(i_q, i_n)	-	(i_q, i_u)	4	12	16
	S_{10}	I_{p-1}	I_{q-4}	I_{0-p}	(i_p, i_w)	-	(i_p, i_m)	-	(i_p, i_w)	-	(i_p, i_v)	-	(i_p, i_w)	0	8	8
	S_{11}	I_{0-p}	I_{0-q}	I_{q-4}	(i_p, i_v)	-	(i_p, i_w)	-	(i_p, i_v)	-	(i_q, i_n)	-	(i_p, i_v)	4	12	16
	S_{12}	I_{q-4}	I_{p-3}	I_{0-p}	(i_p, i_w)	-	(i_p, i_v)	-	(i_p, i_w)	-	(i_q, i_u)	-	(i_p, i_w)	4	12	16
S_M	S_{13}	I_{q-4}	I_{p-3}	I_{0-q}	(i_q, i_n)	-	(i_p, i_v)	-	(i_q, i_n)	-	(i_q, i_u)	-	(i_q, i_n)	4	12	16
	S_{14}	I_{0-p}	I_{0-q}	I_{p-3}	(i_q, i_u)	-	(i_p, i_w)	-	(i_q, i_u)	-	(i_q, i_n)	-	(i_q, i_u)	4	12	16
	S_{15}	I_{p-3}	I_{q-1}	I_{0-q}	(i_q, i_n)	-	(i_q, i_u)	-	(i_q, i_n)	-	(i_q, i_m)	-	(i_q, i_n)	0	8	8
	S_{16}	I_r	I_{s-2}	I_{p-1}	(i_p, i_m)	-	(i_p, i_p)	-	(i_p, i_m)	-	(i_p, i_q)	-	(i_p, i_m)	0	8	8
	S_{17}	I_{p-1}	I_{q-4}	I_{s-2}	(i_p, i_q)	-	(i_p, i_m)	-	(i_p, i_q)	-	(i_p, i_v)	-	(i_p, i_q)	0	8	8
	S_{18}	I_{s-2}	I_{s-1}	I_{q-4}	(i_p, i_v)	-	(i_p, i_q)	-	(i_p, i_v)	-	(i_q, i_p)	-	(i_p, i_v)	4	12	16
	S_{19}	I_{s-2}	I_{s-1}	I_{q-4}	(i_p, i_v)	-	(i_p, i_q)	-	(i_p, i_v)	-	(i_q, i_p)	-	(i_p, i_v)	4	12	16
	S_{20}	I_{q-4}	I_{p-3}	I_{s-2}	(i_p, i_q)	-	(i_p, i_v)	-	(i_p, i_q)	-	(i_q, i_u)	-	(i_p, i_q)	4	12	16
	S_{21}	I_{q-4}	I_{p-3}	I_{s-1}	(i_q, i_p)	-	(i_p, i_v)	-	(i_q, i_p)	-	(i_q, i_u)	-	(i_q, i_p)	4	12	16
	S_{22}	I_{s-2}	I_{s-1}	I_{p-3}	(i_q, i_u)	-	(i_p, i_q)	-	(i_q, i_u)	-	(i_q, i_p)	-	(i_q, i_u)	4	12	16
	S_{23}	I_{s-2}	I_{s-1}	I_{p-3}	(i_q, i_u)	-	(i_p, i_q)	-	(i_q, i_u)	-	(i_q, i_p)	-	(i_q, i_u)	4	12	16
	S_{24}	I_{p-3}	I_{q-1}	I_{s-1}	(i_q, i_p)	-	(i_q, i_u)	-	(i_q, i_p)	-	(i_q, i_m)	-	(i_q, i_p)	0	8	8
	S_{25}	I_{s-1}	I_t	I_{q-1}	(i_q, i_m)	-	(i_q, i_p)	-	(i_q, i_m)	-	(i_q, i_q)	-	(i_q, i_m)	0	8	8

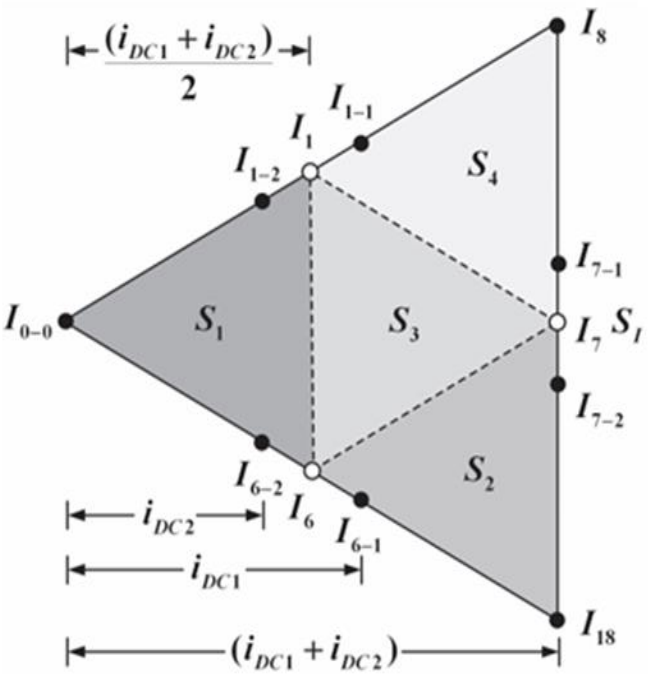

Figure 4: Switching State Vector Alignment

The reference space vector in minor sector S4 is realized with switching state vectors I8, I7−1, I7−2, I1−1, and I1−2, with active periods T8, T7−1 = T7−2 = T7/2, and T1−1 = T1−2 = T1/2, derived from vectors I8, I7, and I1. Similarly, in minor sector S3, vectors I1−1, I1−2, I6−1, I6−2, I7−1, and I7−2 are used, with active periods based on I1, I6, and I7. Table 2 lists all switching vectors per minor sector.

A switching sequence pattern for symmetric waveforms, minimal switch transitions, and balanced switch utilization is developed, as shown in Table 2.

The reference space vector is created by utilizing the nearest switching state vectors for a specific minor sector, such as I6-1, I1-4, and I7-2 in minor sector S17 and I7-2, I7-1, and I1-4 in minor sector S18.

Table 2: Sector-Based Switching State Vectors in Method 2

Major sector	Minor sector	Switching state vector position			Switching state vectors			Switching states sequence							Number of switch transitions		
		x	y	z	x	y	z	$\frac{T_z}{4}$	$\frac{T_x}{2}$	$\frac{T_y}{2}$	$\frac{T_z}{2}$	$\frac{T_x}{2}$	$\frac{T_y}{2}$	$\frac{T_z}{4}$	CFI-1	CFI-2	Total
S_M	S_1	I_p	I_q	I_0	I_{p-1} and I_{p-2}	I_{q-1} and I_{q-2}	I_{0-0}	(i_m, i_m)	(i_p, i_m)	(i_q, i_m)	(i_m, i_m)	(i_m, i_p)	(i_m, i_q)	(i_m, i_m)	6	6	12
	S_2	I_r	I_s	I_p	I_r	I_{s-1} and I_{s-2}	I_{p-1} and I_{p-2}	(i_p, i_m)	(i_p, i_p)	(i_q, i_p)	(i_m, i_p)	(i_p, i_p)	(i_p, i_q)	(i_p, i_m)	6	6	12
	S_3	I_p	I_q	I_s	I_{p-1} and I_{p-2}	I_{q-1} and I_{q-2}	I_{s-1} and I_{s-2}	(i_p, i_q)	(i_p, i_m)	(i_q, i_m)	(i_q, i_p)	(i_m, i_p)	(i_m, i_q)	(i_p, i_q)	6	6	12
	S_4	I_s	I_t	I_q	I_{s-1} and I_{s-2}	I_t	I_{q-1} and I_{q-2}	(i_q, i_m)	(i_q, i_p)	(i_q, i_q)	(i_m, i_q)	(i_p, i_q)	(i_q, i_q)	(i_q, i_m)	6	6	12

IV SIMULATION RESULTS

Method 1 shows that the current ia, which includes intermediate current levels, significantly reduces low-frequency harmonic components, as shown in Fig. 5(a), and the Figures 5(b) and 5(c) phase-a current for CFI-1 and CFI-2.

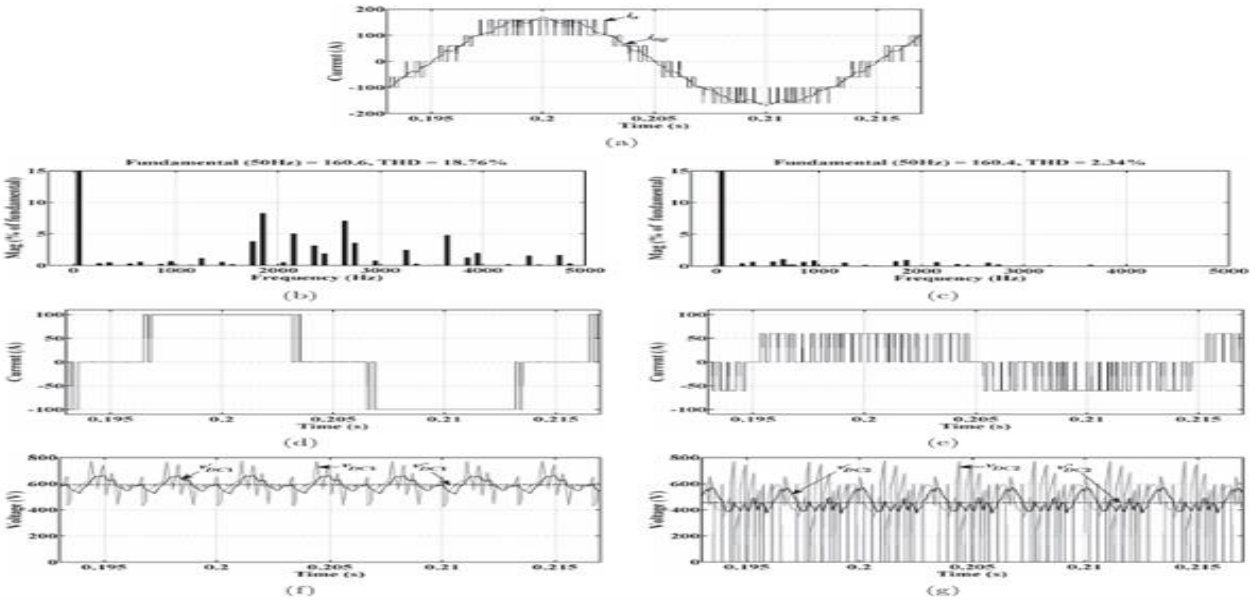

Figure 5: Simulation Results for Method-1 with I_{dc1}=100 A and I_{dc2}=60 A: (a) Output Current I_a and Grid Current I_{ag} (b) Harmonic Spectrum of Output Current I_a (c) Harmonic Spectrum of Grid Current I_{ag} (d) Phase-A Current I_{a1} for CFI-1 (e) Phase-A Current I_{a2} for CFI-2 (f) DC-Link Voltage V_{dc1} for CFI-1 (g) DC-Link Voltage V_{dc2} for CFI-2

Method 2 selects specific switching state vectors to eliminate low-frequency pulsations in DC-link voltages of CFIs, stabilizing DC-link voltage for complex, high-performance inverter systems, as shown in simulation results. in fig. 6

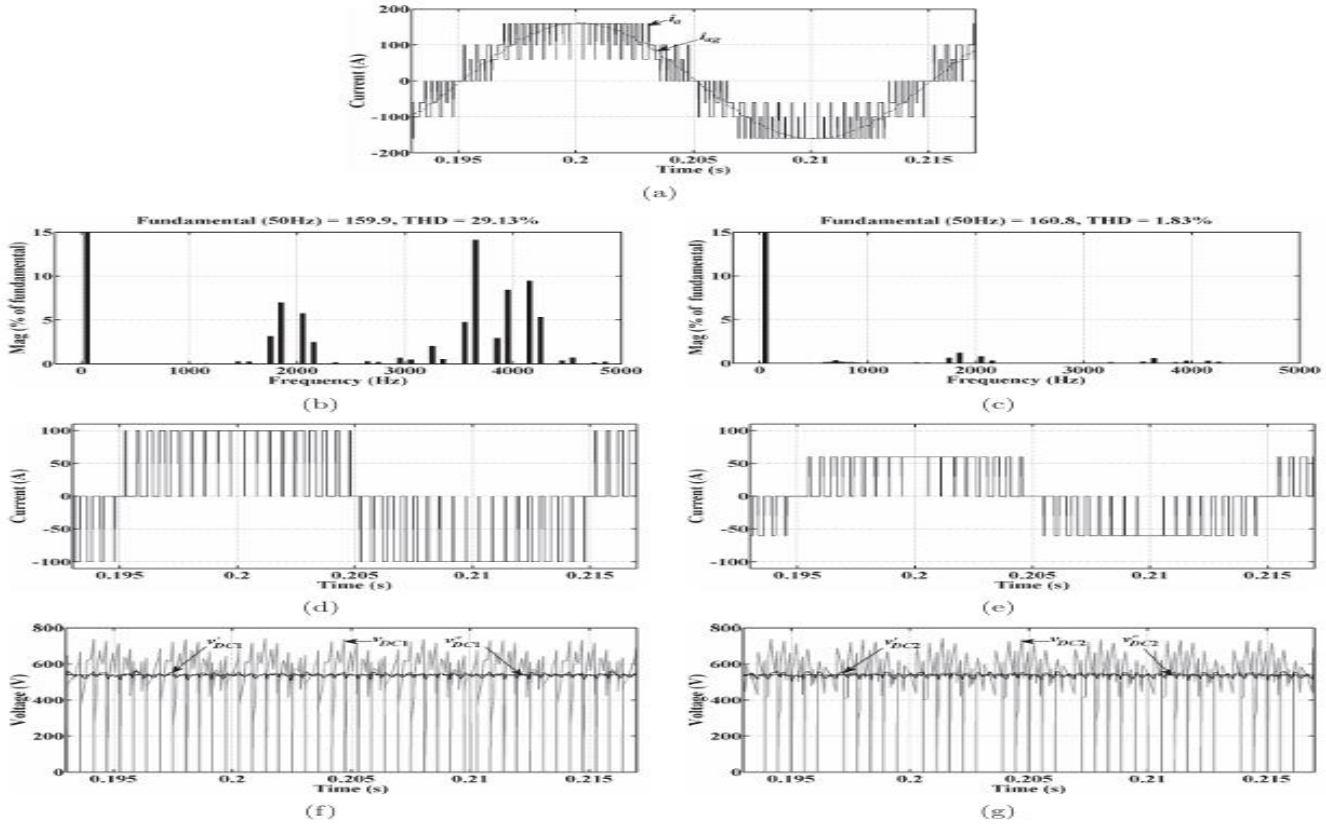

Figure 6: Simulation results for Method-2: i_{DC1} = 100 A and i_{DC2} = 60 A (a) Output Current ia and Grid Current iag (b) Harmonic Spectrum of Output Current ia (c) Harmonic Spectrum of Grid Current iag (d) Phase-a Current i_{a1} for CFI-1 (e) Phase-a Current i_{a2} for CFI-2 (f) DC-link Voltage V_{DC1} for CFI-1 (g) DC-link Voltage V_{DC2} for CFI-2

V CONCLUSION

Two methods using SVM technique are used to select switching state vectors in multilevel current-fed inverters (CFIs) to eliminate low-frequency harmonic components in output currents, particularly under unequal dc-link current conditions.

Method 1 creates a reference current space vector using nearest switching state vectors in minor sectors, allowing higher current inverters to operate at lower frequencies, improving efficiency. However, this method has low-frequency pulsations in DC-link voltage and requires careful design of DC-DC converters to accommodate output voltage variations due to inequality in DC-link currents.

Method 2 selects switching state vectors to eliminate low-frequency pulsations in CFI DC-link voltages, reducing computational burden and extending principles to systems with multiple parallel CFI units, and reduces the computational burden of identifying the operating sector and calculating duty cycles.

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